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NOTES:  
1.HSF Property:Comply iSupplier system HSF property attribute up-to-date value.

A10  
REFRESH  
SVT BUILD

2019.04.08

03-Oct-2019		
DATE	CHANGING	REV

DESIGN / DRAWER	XXX	DATE	03-Oct-2019	TITLE A10			
CHECK	BRYAN CHIOU			SIZE	A1	COLL	G
APPROVAL	TICKY TSAI			DOC NUMBER	1310xxxxx-0-0	REV	A02
FILENAME	A10_SQVP			SHEET	of 20		
PCB PIN	60xxxxxxxxxxx	PCB VER	A02				

INVENTEC

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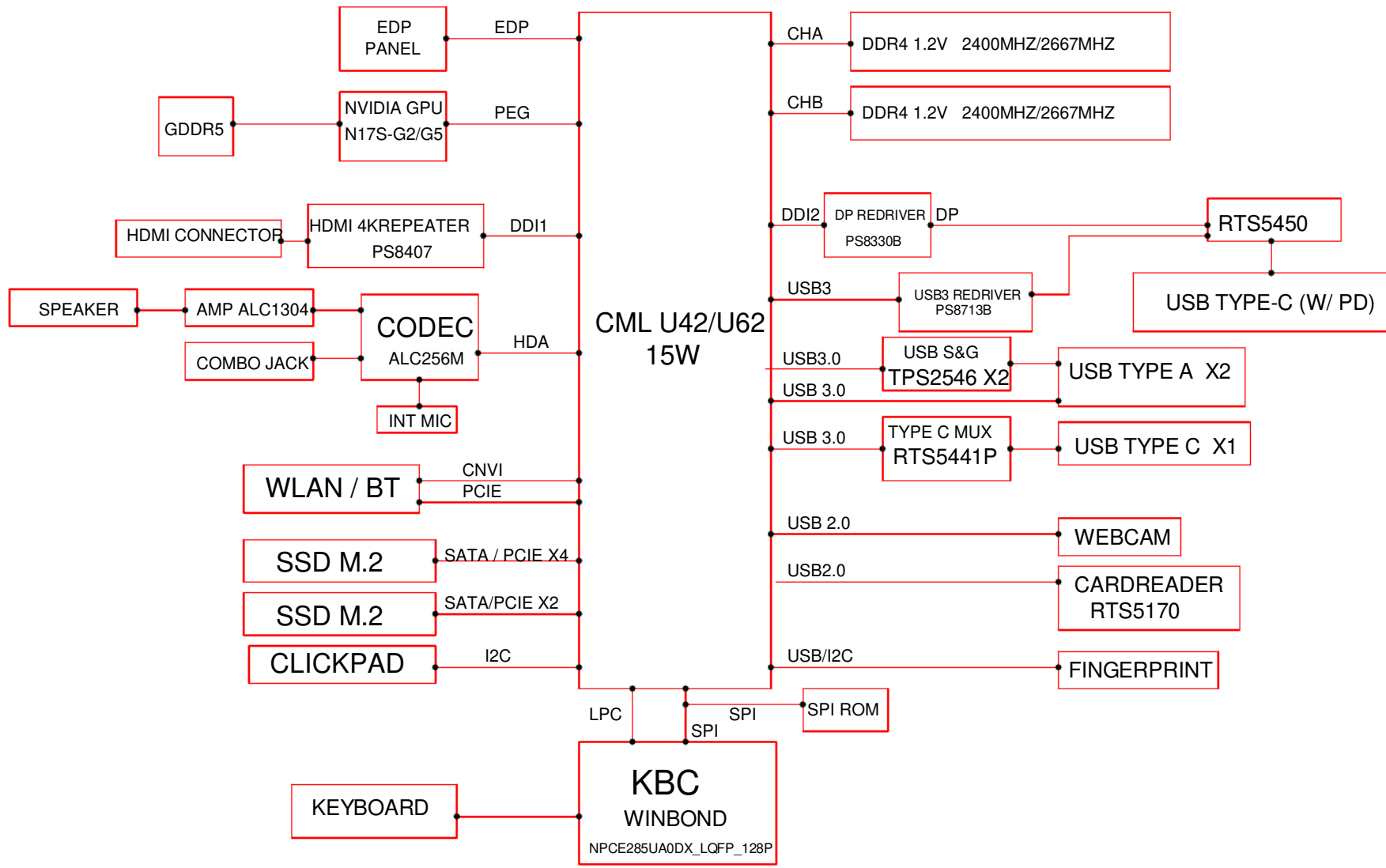
23 CPU-DDR  
24 CPU-LPC, SPI, SMBUS, CLINK  
25 CPU-GPIO  
26 CPU-MISC, HDA, SDIO, JTAG  
27 CPU-PCIE, USB3, USB2  
28 CPU-CLK, RTC, CFG  
29 CPU-DDI, EDP, CSI2, EMMC  
30 CPU-POWER MANAGEMENT  
31 CPU-POWER1  
32 CPU-POWER2  
33 CPU-POWER3  
34 CPU-GND, CFG, RSVD  
35 EC\_NPCE285  
36 KB\_CONN & LED  
37 TOUCH\_CONN/LID SWITCH  
38 CODEC ALC256M  
39 AUDIO JACK  
40 AMP ALC1304  
41 CARDREADER RTS5170  
42 USB3.0 CONN1  
43 USB3.0 CONN2  
44 USB3 REDRIVER  
45 TYPE C RTS5441P  
46 TYPE C CONN1  
47 WLAN ON BOARD  
48 NGFF\_M.2 SSD1

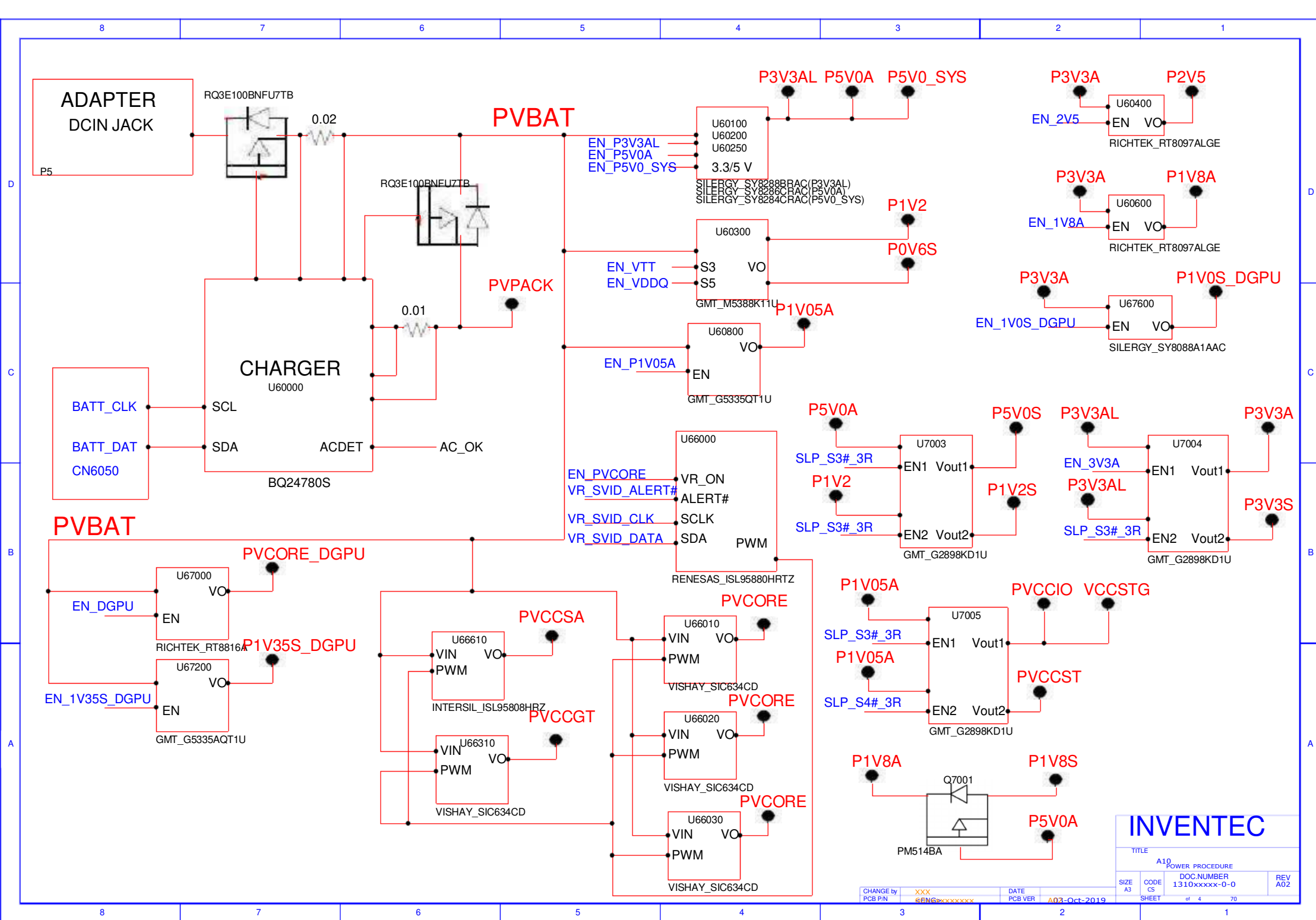
49 NGFF M.2 SSD2  
50 DP REDRIVER  
51 USB3 REDRIVER  
52 TYPE C RTS5450  
53 TYPE C CONN2  
54 EDP CN  
55 CAMERA  
56 FAN  
57 HDMI 4K\2K  
58 HDMI CONN  
59 GPU COVER  
60 GPU-1  
61 GPU-2  
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63 GPU-4  
64 GPU-5  
65 GDDR5 VRAM  
66 DGPU\_RT8816A  
67 DGPU\_P1V35  
68 DGPU\_P1V0S  
69 GPU POWER SEQUENCE  
70 RF&EMI

INVENTEC

TITLE		A10	
INDEX			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	A02
SHEET		of 2	70

CHANGE by	XXX	DATE	03-Oct-2019
PCB PIN	6880xxxxxx	PCB VER	A02





**CHARGER**

DON'T PUT ANY CAPACITOR

SPECIAL CASE, PLEASE CHECK CN60050 PIN 1

**INVENTEC**

TITLE: A10 Block Diagram  
 SIZE: A3  
 CODE: CS  
 SHEET: 5 of 70  
 DOC NUMBER: 1310xxxxx-0-0  
 REV: A02  
 CHANGE by: XXX  
 PCB P/N: 60xxxxxxxxxx  
 DATE: 03-Oct-2019  
 PCB VER: A02

**CHARGER**

DON'T PUT ANY CAPACITOR

PVADPTR

Q60010 PE534BA

Q60011 NEMOS\_PE528BA

Q60012 PE534BA

U60000

TI\_BQ24780S\_QFN\_28R

P3V3\_LDO

PVBAT

PVPACK

INVENTEC

CHANGE by XXX  
PCB P/N 60xxxxxxxxxx

DATE 03-Oct-2019  
PCB VER A02

DOC NUMBER 1310xxxxxx-0-0

REV A02

SHEET 5 of 70

**CHARGER**

DON'T PUT ANY CAPACITOR

PVADPTR

Q60010 PE534BA

Q60011 NEMOS\_PE528BA

Q60012 PE534BA

U60000

TI\_BQ24780S\_QFN\_28R

P3V3\_LDO

PVBAT

PVPACK

INVENTEC

CHANGE by XXX  
PCB P/N 60xxxxxxxxxx

DATE 03-Oct-2019  
PCB VER A02

DOC NUMBER 1310xxxxx-0-0

REV A02

SHEET 5 of 70

**CHARGER**

DON'T PUT ANY CAPACITOR

PVADPTR

Q60010 PE534BA

Q60011 NEMOS\_PE528BA

Q60012 PE534BA

U60000

TI\_BQ24780S\_QFN\_28R

P3V3\_LDO

PVBAT

PVPACK

INVENTEC

CHANGE by XXX PCB P/N 60XXXXXXXXXX DATE PCB VER 03-Oct-2019 A02

SHEET 5 of 70

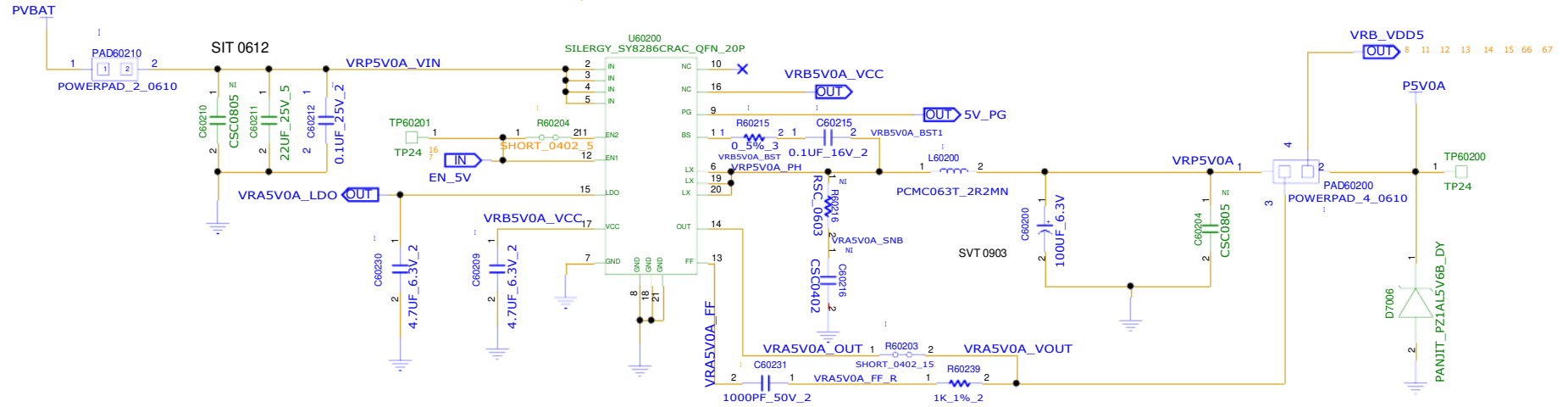
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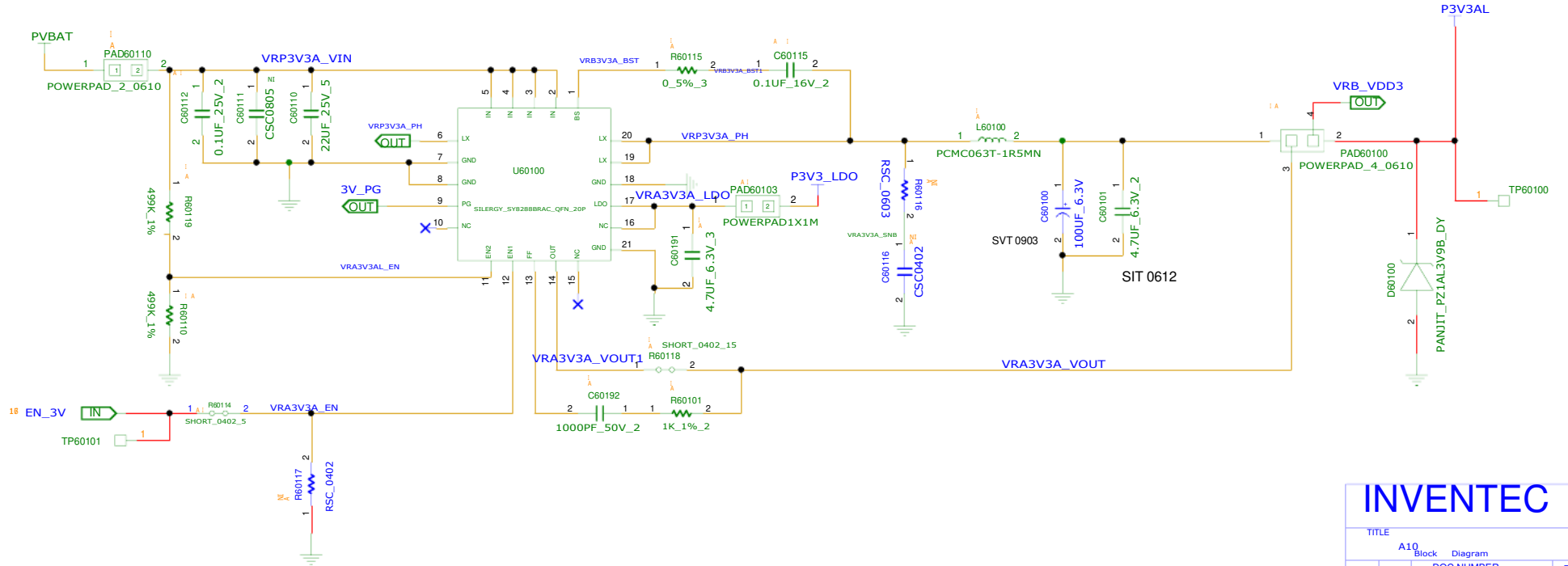
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TITLE A10 Block Diagram

# P5V0A



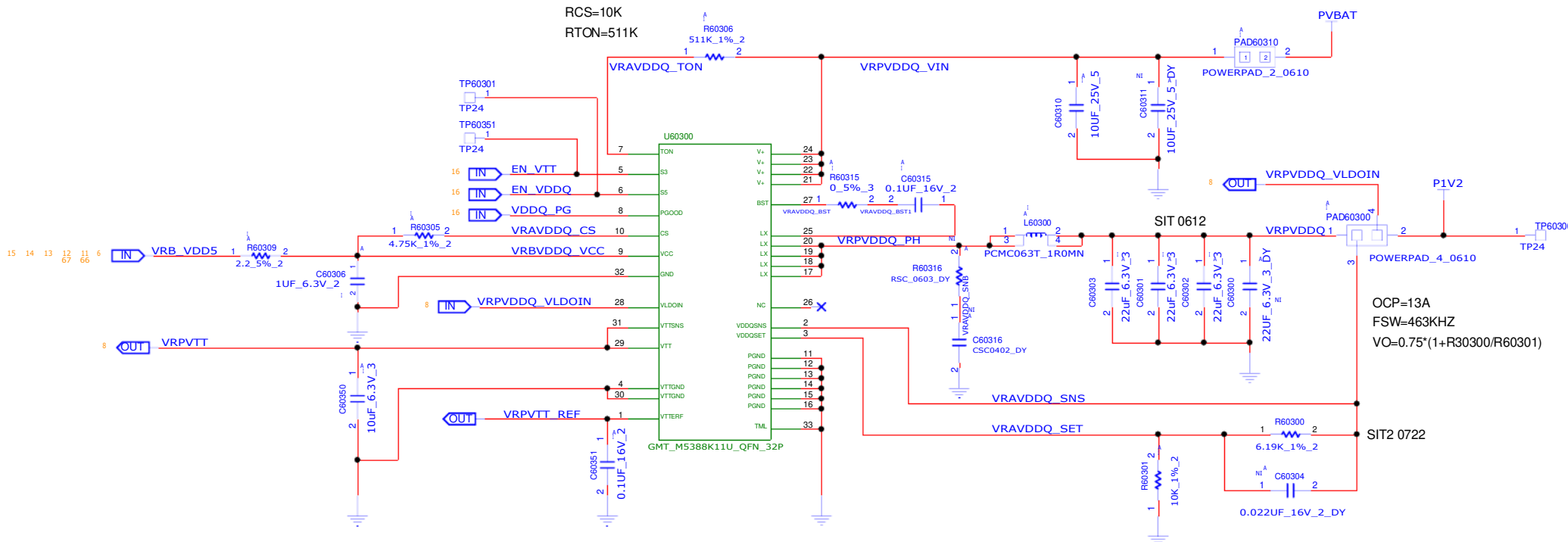
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INVENTEC

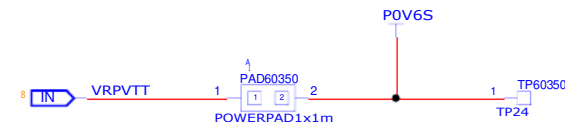


## DDR POWER



**Table 2. S3 and S5 Control Table**

STATE	S3	S5	VTT	VTTREF
Normal	Hi	Hi	VTTREF	VDDQSNS/2
Standby	Lo	Hi	OFF (High-Z)	VDDQSNS/2
Shutdown	Lo	Lo	0V (Discharge)	0V (Discharge)



# INVENTEC

TITLE	A10	Block	Diagram
-------	-----	-------	---------

SIZE	CODE	DOC.NUMBER
		1310xxxxx-0-0

A3	CS	1510000
SHEET		8 of 70

REV  
A02

<b>CHANGE by</b>	<b>XXX</b>	<b>DATE</b>	<b>03-Oct-2019</b>
<b>PCB R/N</b>	<b>60.....</b>	<b>PCB VER</b>	<b>A02</b>



D



C

B

A

TITLE
A10 Block Diagram

---

8

7

6

5

4

1

1

1

D



B

A

D

C

B

A

D

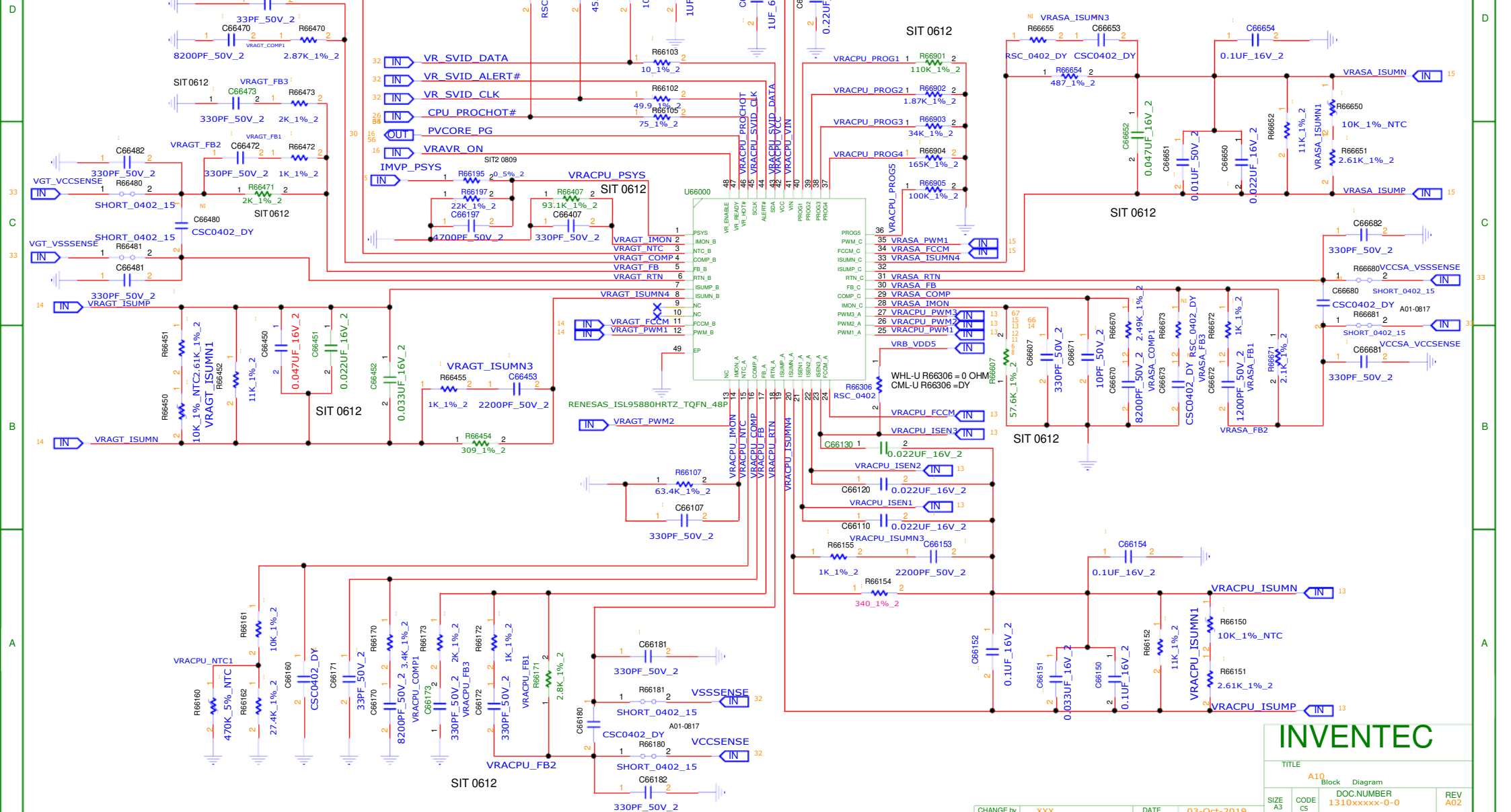


B

A

8	7	6	5	4	3	2	1
---	---	---	---	---	---	---	---

## CONTROLLER



# INVENTEC

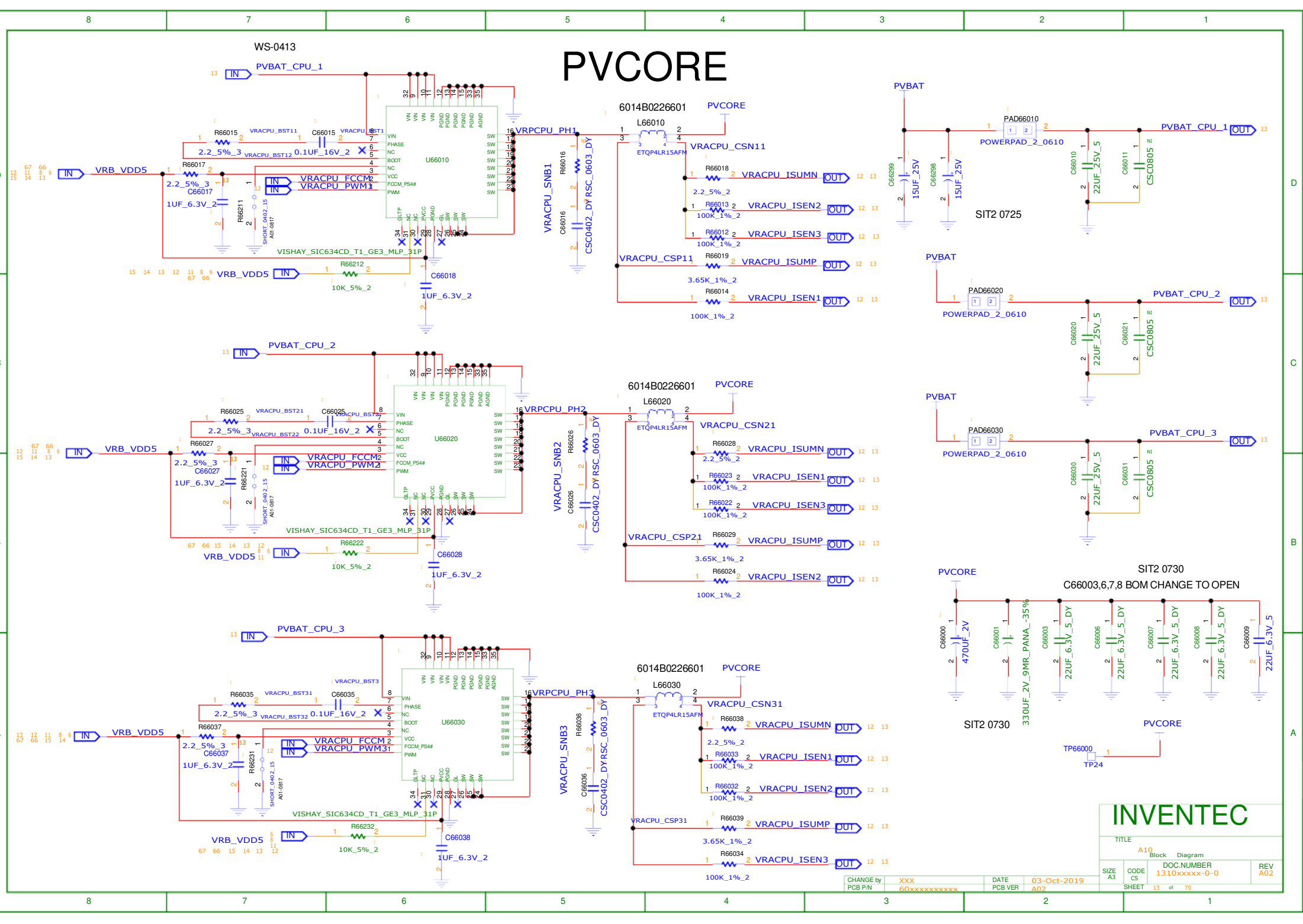
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SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A02
SHEET		12 of 70	

CHANGE by	XXX
PCB P/N	60xxxxxxxxxxxx

DATE	03-Oct-2019
PCB VER	A03

SIZE A3	CODE CS	1310xxxxx-0-0	A02
	SHEET	12 of 70	

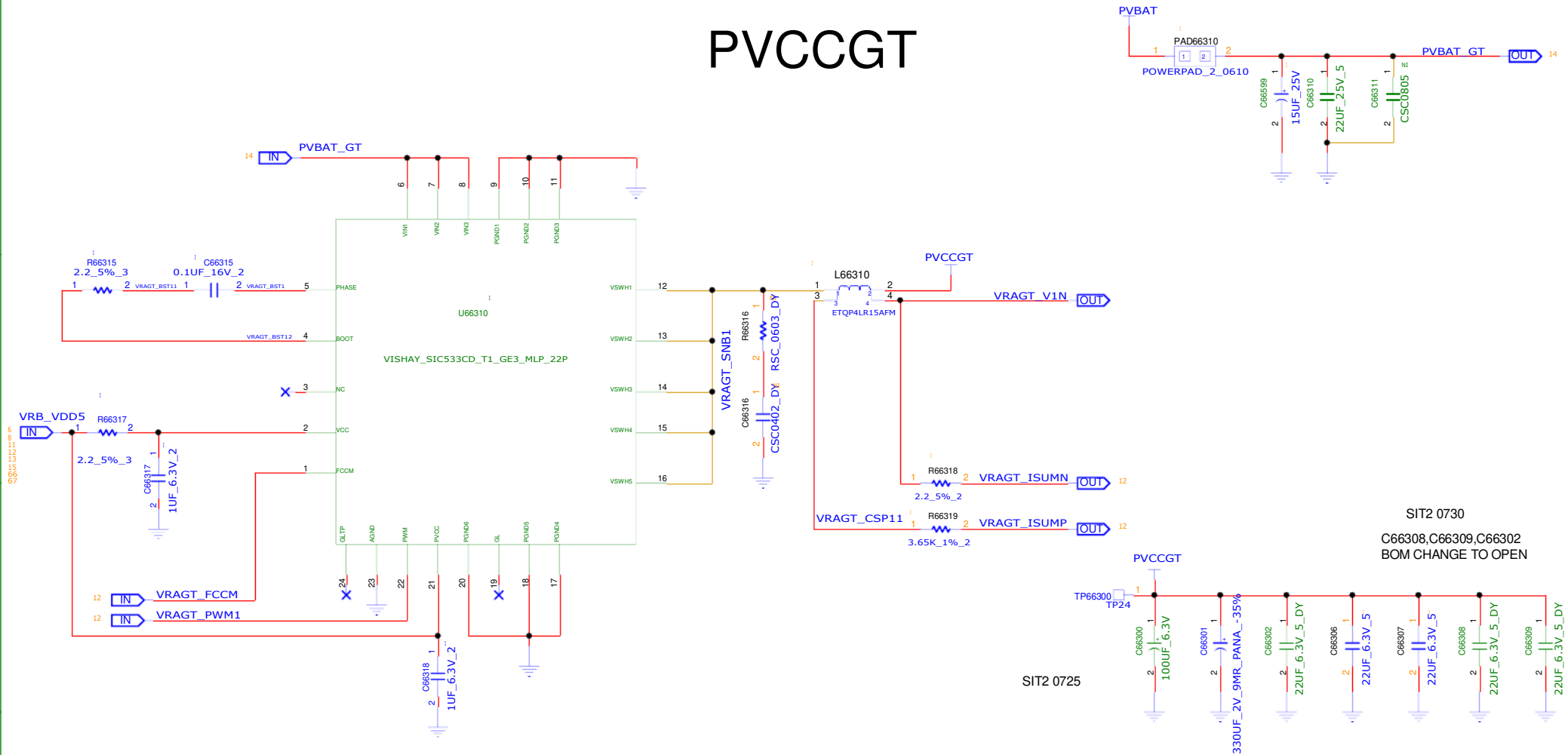
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INVENTEC				
TITLE				
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SIZE	CODE	DOC NUMBER		
A3	CS	1310xxxx-0-0		
SHEET		13 of 70		
REV		A02		

CHANGE by	XXX	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	A02

PVCCGT

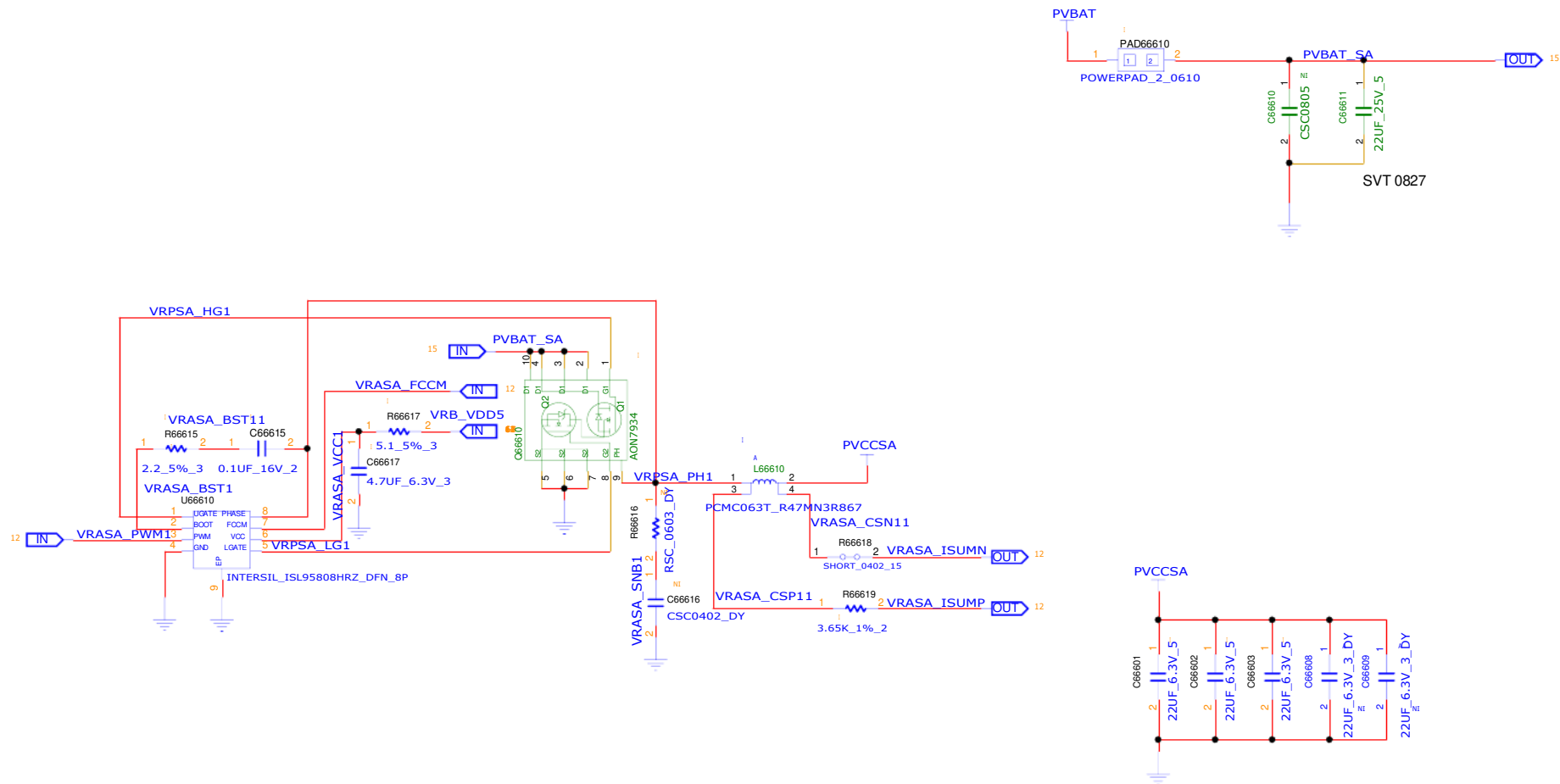


# INVENTEC

TITLE			
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SIZE A3	CODE CS	DOC.NUMBER 1310xxxx-0-0	REV A02
SHEET		14 of 70	

CHANGE by	XXX	DATE	03-Oct-2019	SIZE	A3	CODE	CS	1310xxxxx-0-0	A02
PCB P/N	60xxxxxxxxxx	PCB VER	A02	SHEET	14	of	70		

# PVCCSA

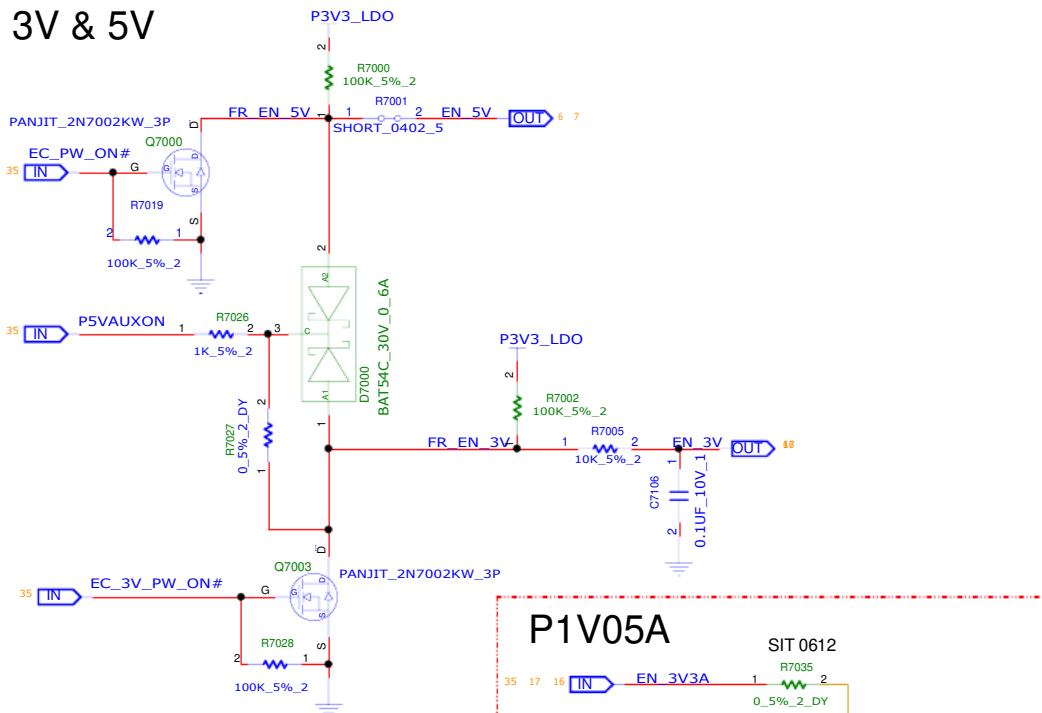


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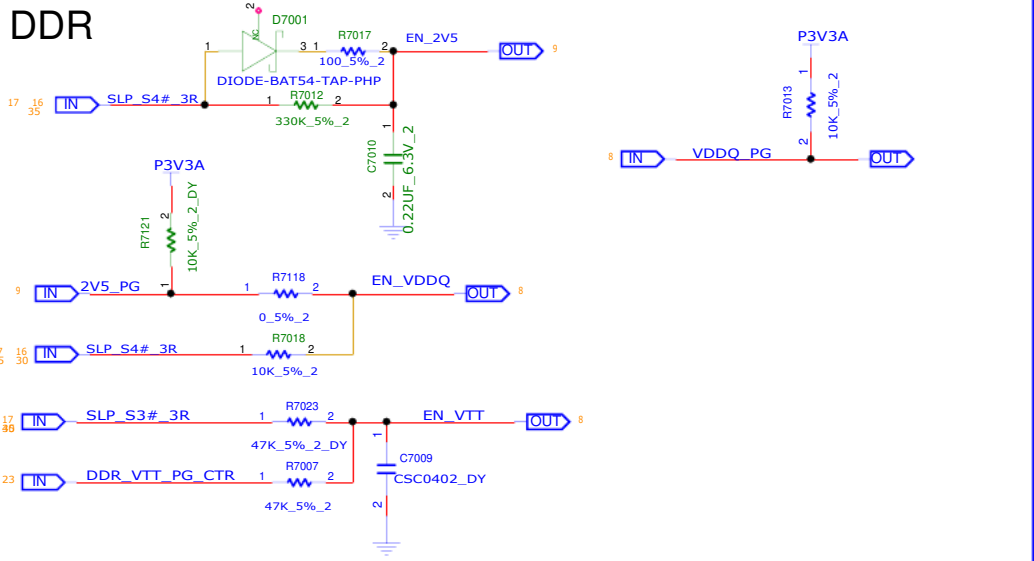
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SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A02
SHEET		15 of 70	

CHANGE by	XXX	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	A02

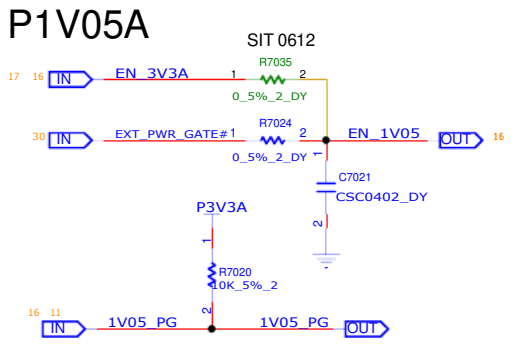
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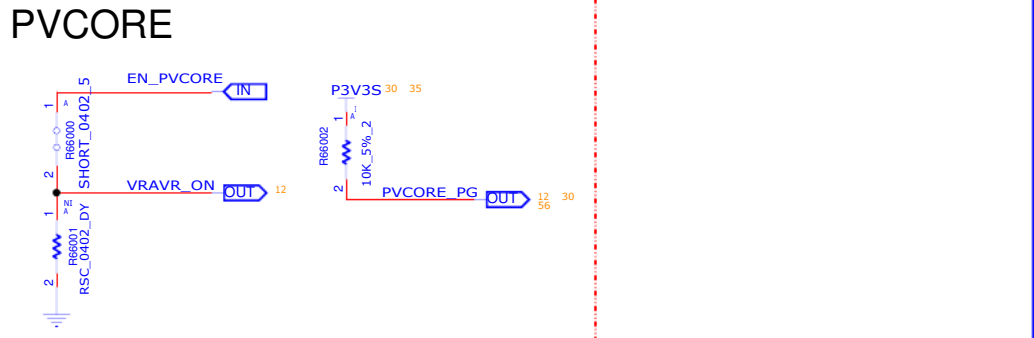
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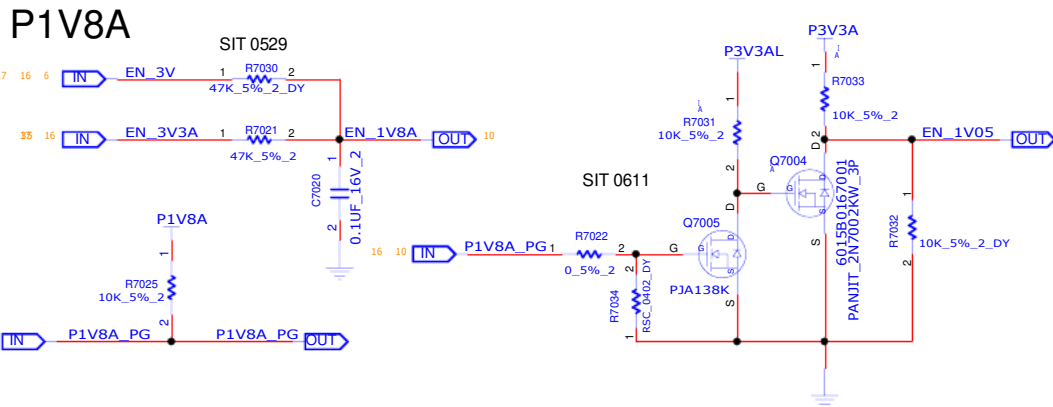
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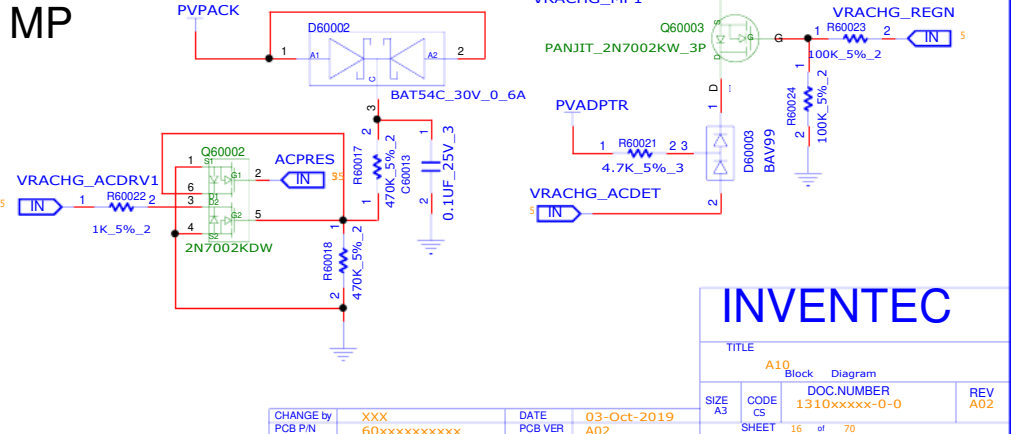
# PVCORE



# P1V8A



# MP

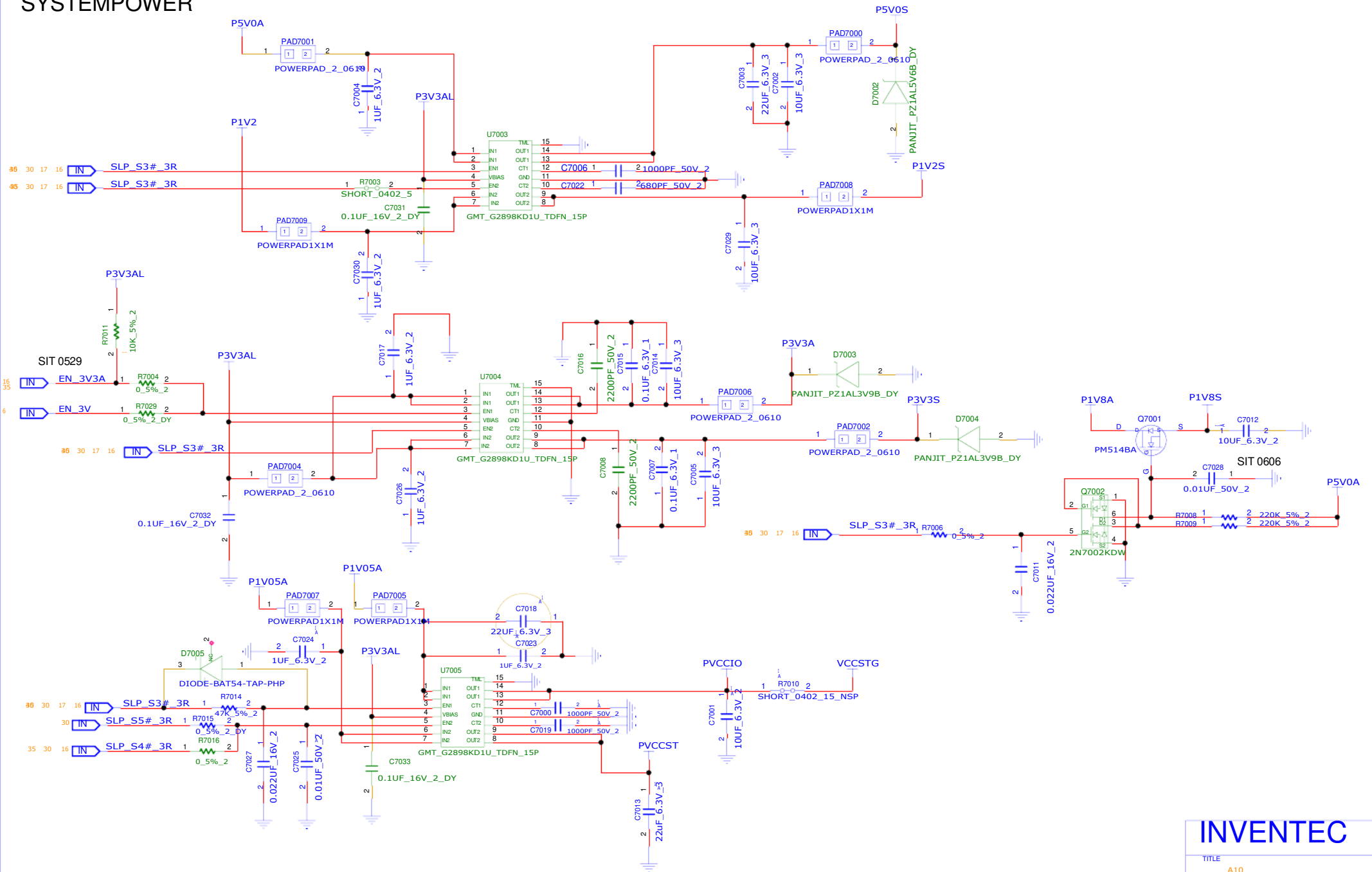


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CHANGE by	XXX	DATE	03-Oct-2019	TITLE	A10 Block Diagram	REV	A02
PCB P/N	60xxxxxxxxxx	PCB VER	A02	CODE CS	1310xxxx-0-0	SHEET	16 of 70



# SYSTEMPOWER

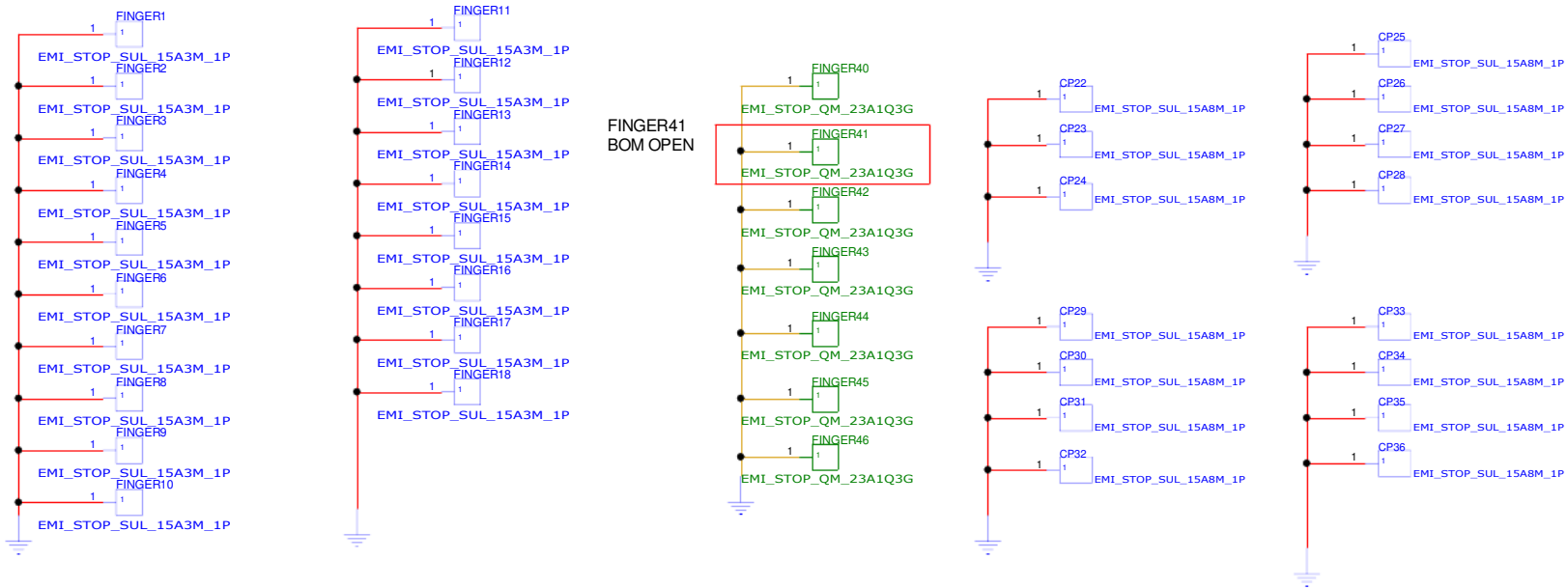


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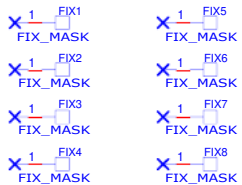
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SHEET 17 of 70			

CHANGE by	XXX	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	A02

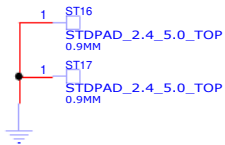
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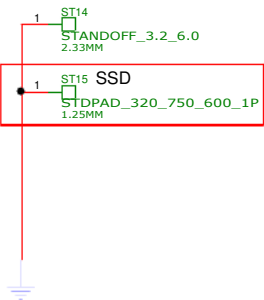
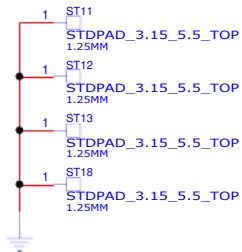
FINGER41  
BOM OPEN



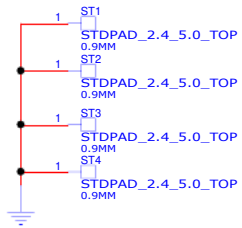
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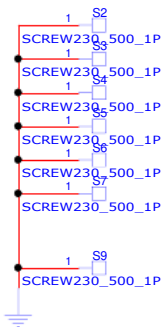
FAN



CPU



PCB

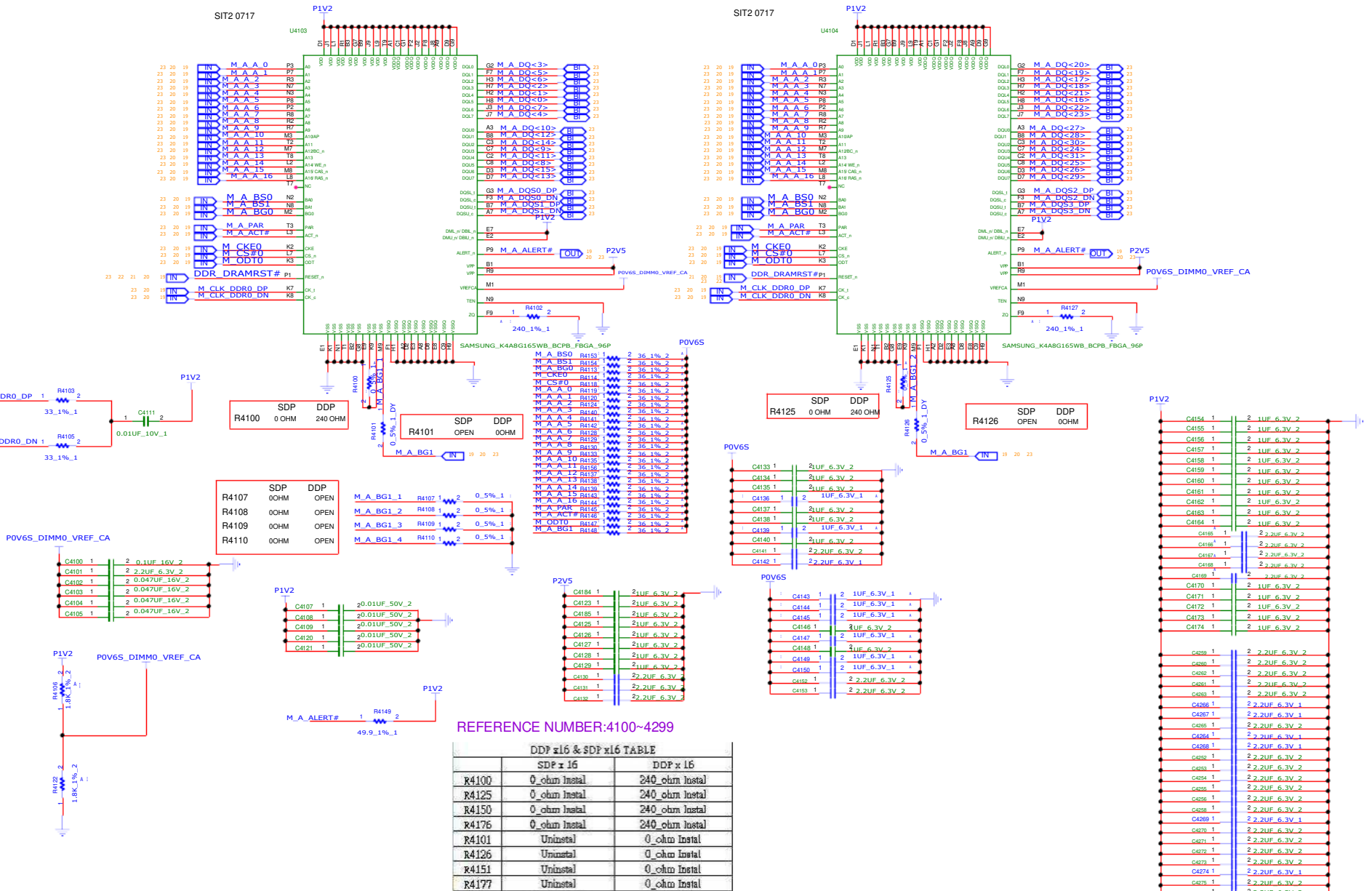


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TITLE			
A10 Block Diagram			
SIZE	CODE	DOC NUMBER	REV
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SHEET	18	of 70	

CHANGE by	XXX	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	A02

# DDR4



REFERENCE NUMBER:4100-4299

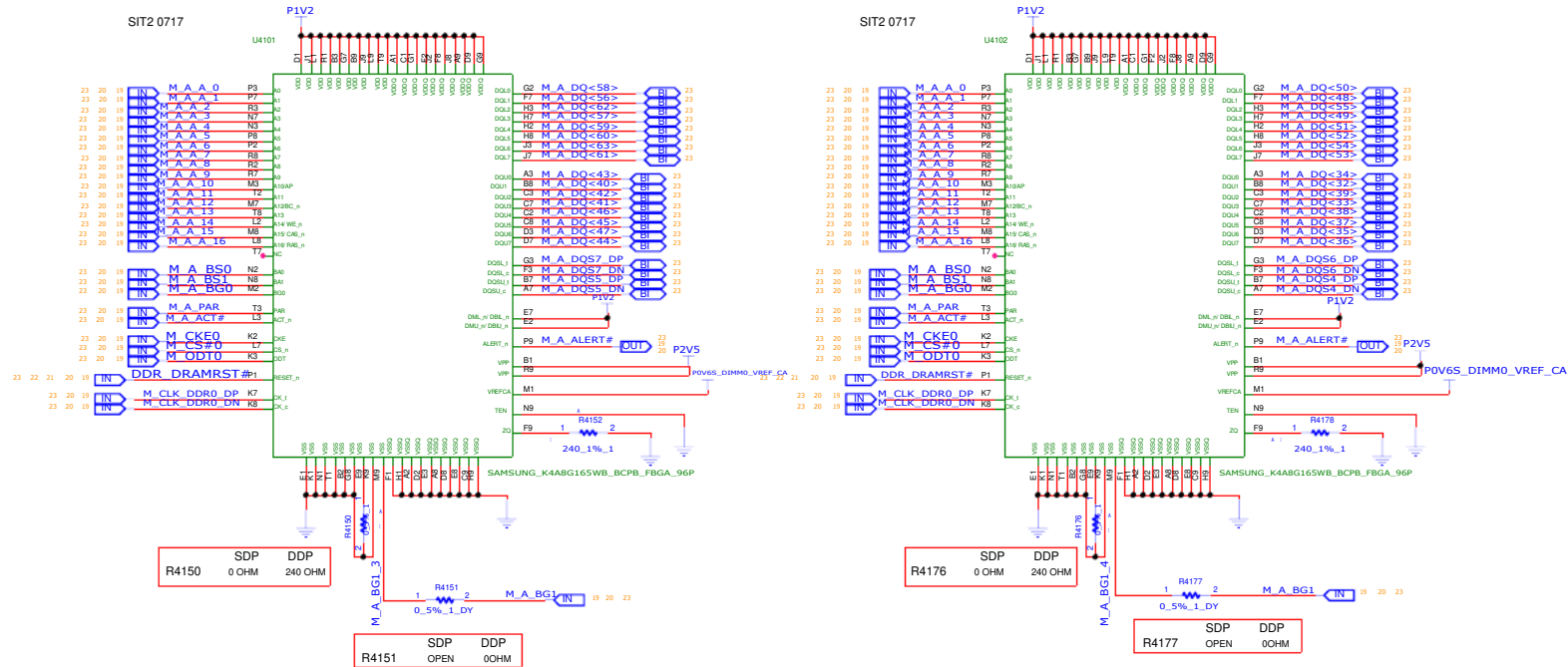
DDR x16 & SDP x16 TABLE		
	SDP x16	DDP x16
R4100	0_ohm Instal	240_ohm Instal
R4125	0_ohm Instal	240_ohm Instal
R4150	0_ohm Instal	240_ohm Instal
R4176	0_ohm Instal	240_ohm Instal
R4101	Uninstal	0_ohm Instal
R4126	Uninstal	0_ohm Instal
R4151	Uninstal	0_ohm Instal
R4177	Uninstal	0_ohm Instal
R4107	0_ohm Instal	Uninstal
R4108	0_ohm Instal	Uninstal
R4109	0_ohm Instal	Uninstal
R4110	0_ohm Instal	Uninstal

INVENTEC

TITLE	A10	Block	Diagram
SIZE	A1	CDE	DOC NUMBER
SHEET	13	REV	A02

CHANGE BY: XXX PCB PIN: 0000000000 DATE: 03-Oct-2019 PCB VER: A02

# DDR4

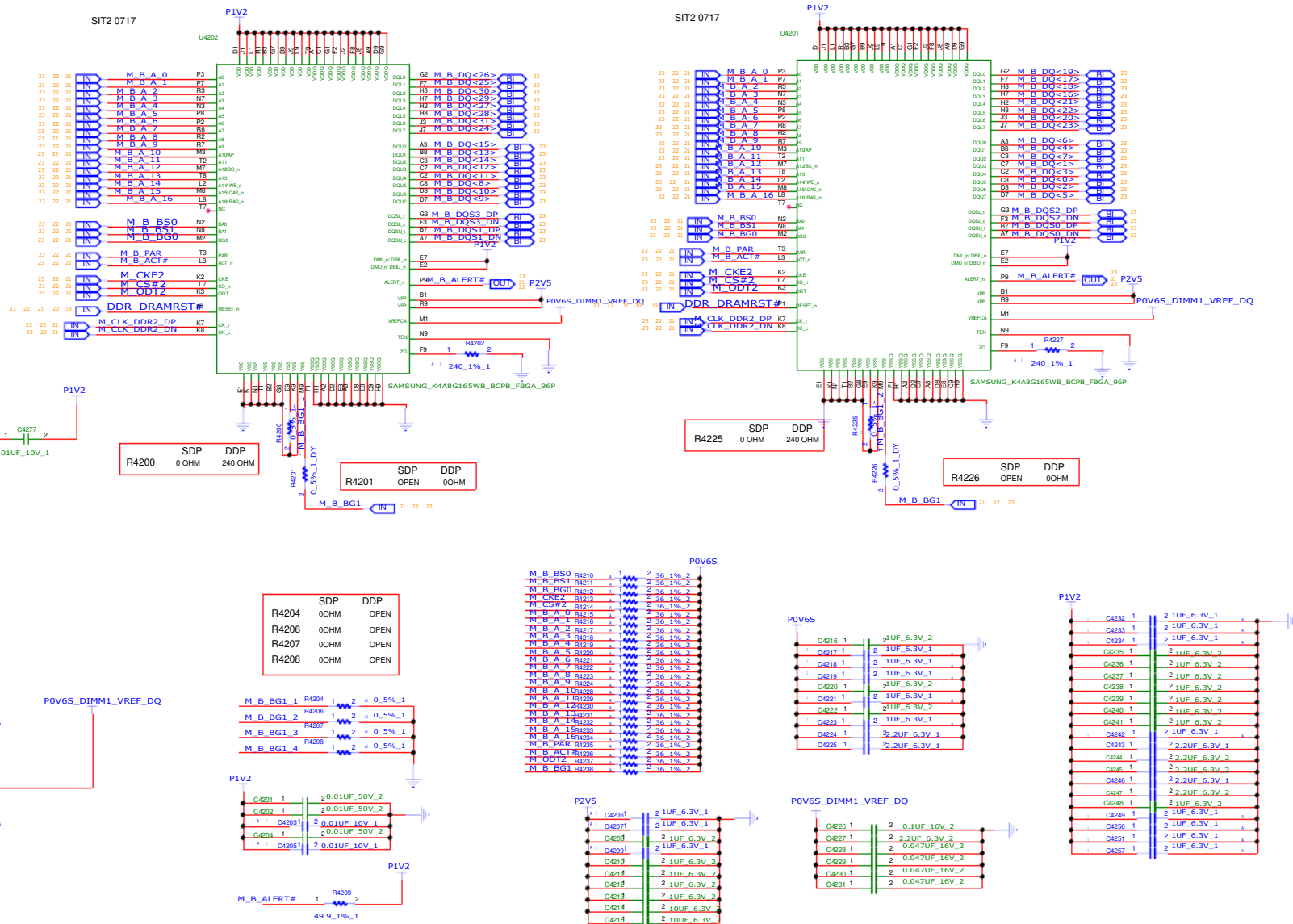


DDP x16 & SDP x16 TABLE		
	SDP x 16	DDF x 16
R4100	0_ohm Instal	240_ohm Instal
R4125	0_ohm Instal	240_ohm Instal
R4150	0_ohm Instal	240_ohm Instal
R4176	0_ohm Instal	240_ohm Instal
R4101	Uninstal	0_ohm Instal
R4126	Uninstal	0_ohm Instal
R4151	Uninstal	0_ohm Instal
R4177	Uninstal	0_ohm Instal
R4107	0_ohm Instal	Uninstal
R4108	0_ohm Instal	Uninstal
R4109	0_ohm Instal	Uninstal
R4110	0_ohm Instal	Uninstal

REFERENCE NUMBER:4100~4299

INVENTEC

# DDR4

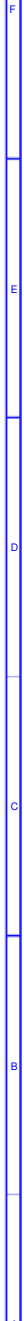


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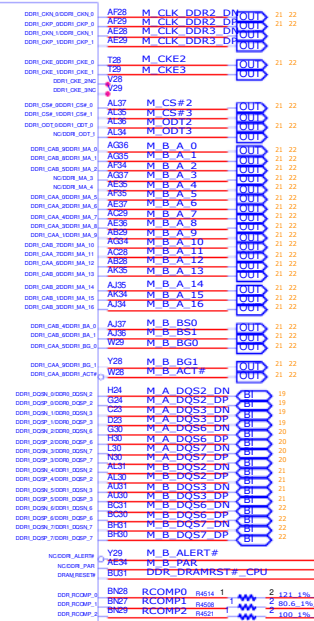
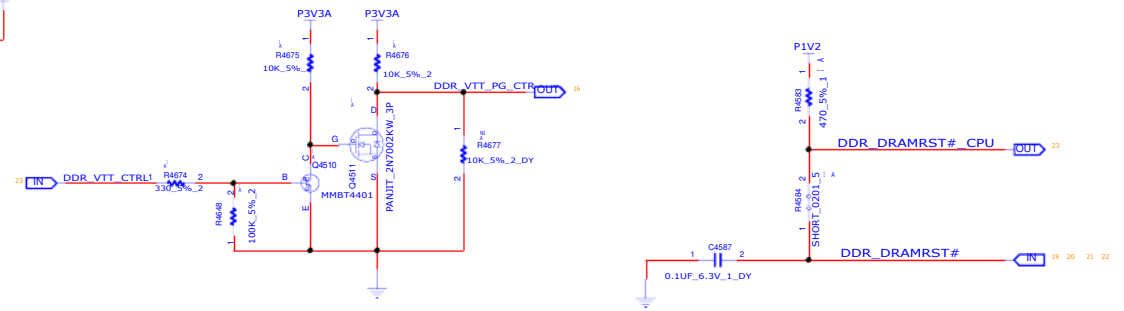
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A10		Block		C5		03-Oct-2019		A02	
SIZE		CODE		DOC NUMBER		1310xxxx-0-0		REV	
PCB PIN		SHEET		21		20			

	F
	E
	D
	C
	B
	A



1

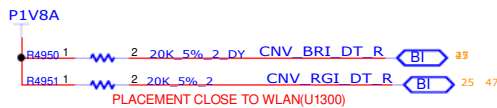
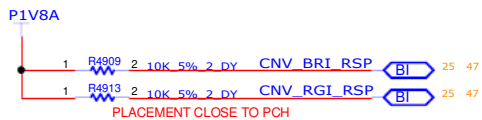
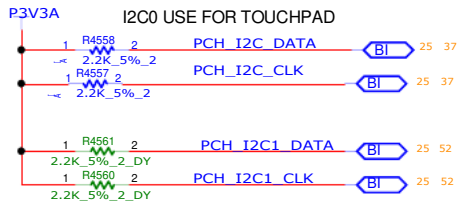
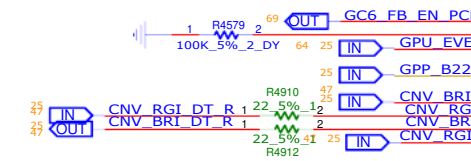
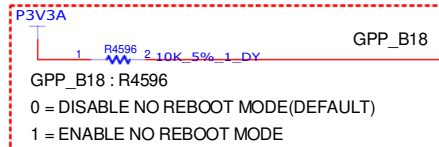
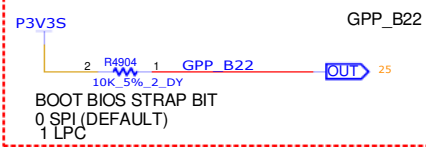
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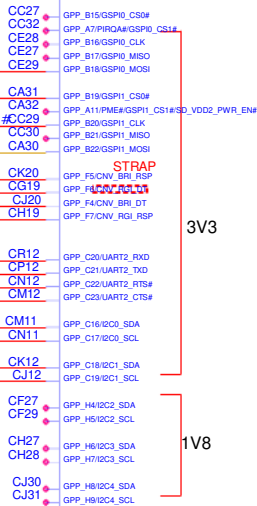




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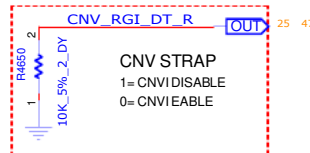


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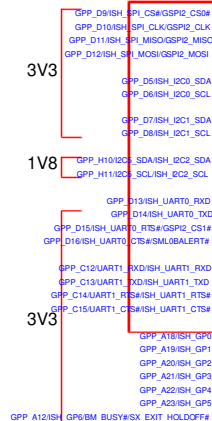
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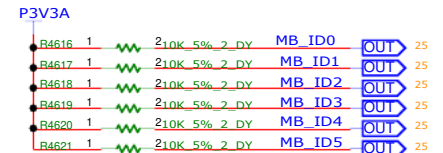
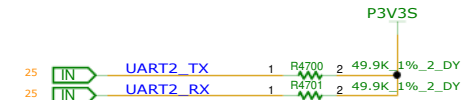
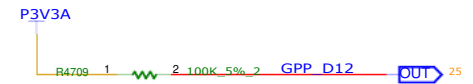


CNV RGI\_DT PIN GETS THE PULL-DOWN RESISTOR (1K OHM) FROM THE INTERNAL CRF MODULE WHEN CNVI IS ENABLED. THERE MUST NOT BE ANY PULL-DOWN RESISTOR CONNECTED ON THE BOARD.

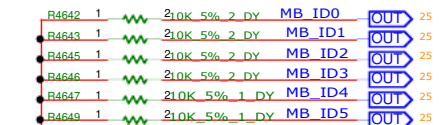
## INTEGRATED SENSOR HUB



Vendor	Part No.	Revision	MS ID0	MS ID1
Samsung	K4A4G32EWC-BCTD	6X09B19Z001	803	0
Samsung	K4A4G32EWA-BCTD	6X09B19Z001	1603	0
Hynix	H5A4G32ANC-BYEC	6X09B19Z001	803	1
Hynix	H5A4G32ANC-BYEC	6X09B19Z001	1603	1



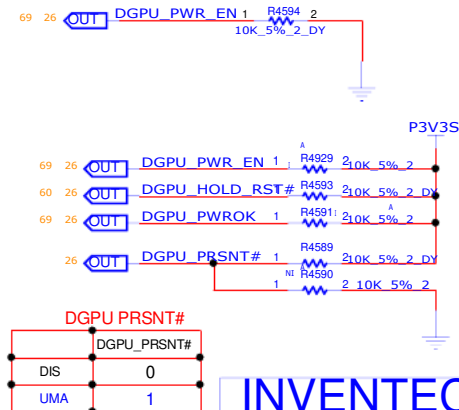
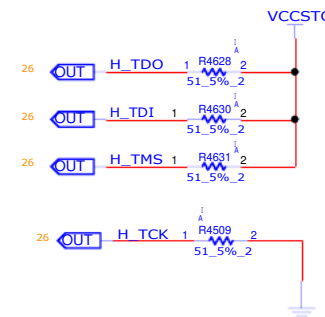
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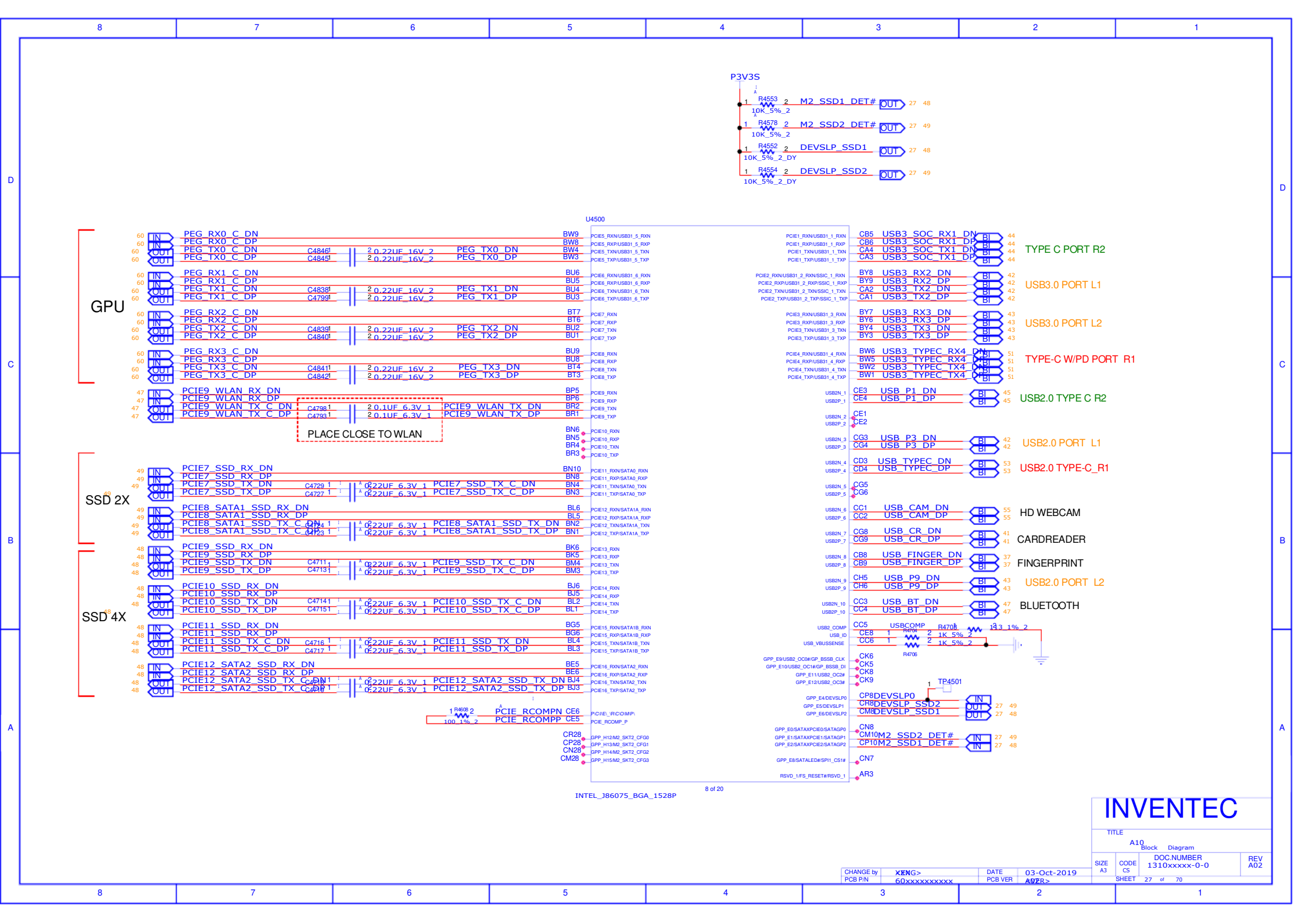


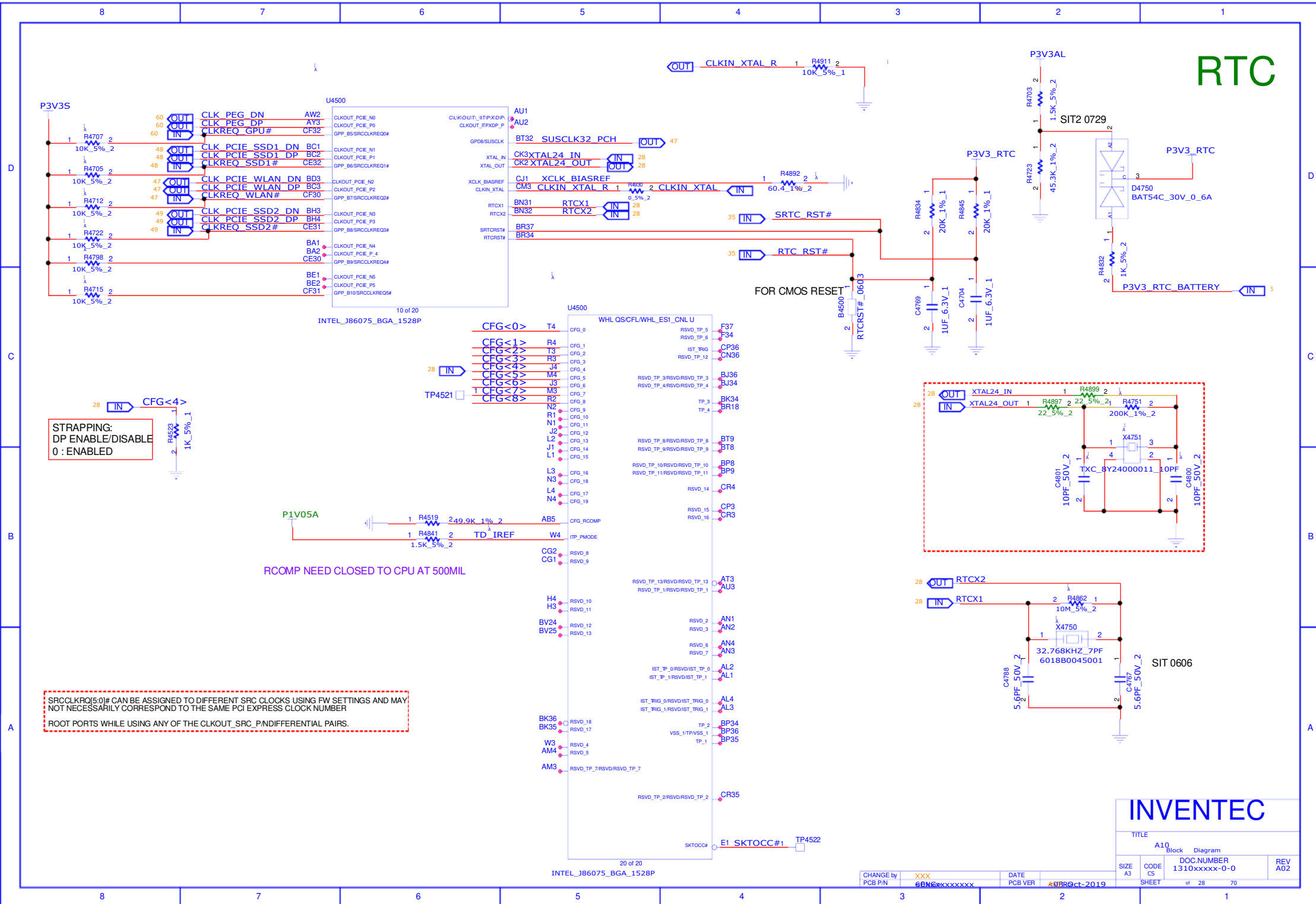
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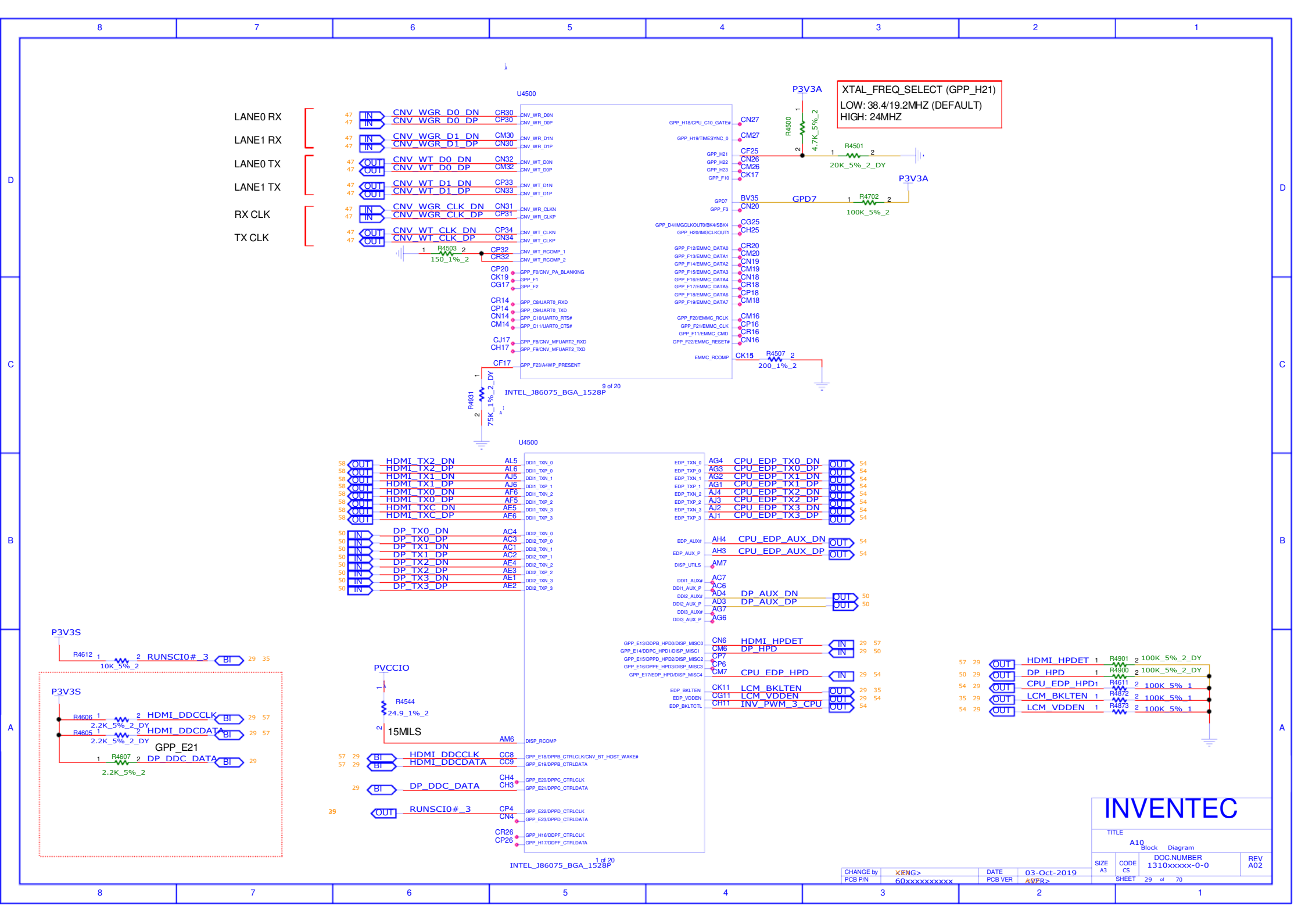
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SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxxx-0-0	A02
SHEET		25	of 70

CHANGE by	XKMG>	DATE	03-Oct-2019
PCB P/N	60xxxxxxx	PCB VER	A02R>







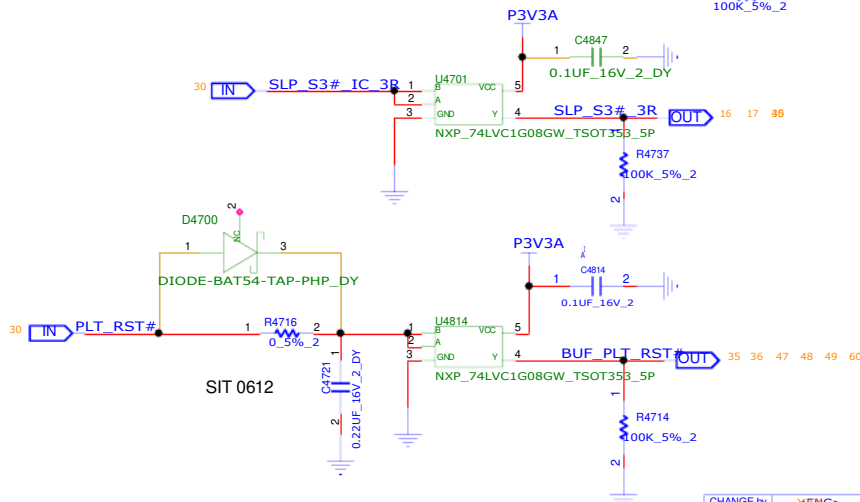
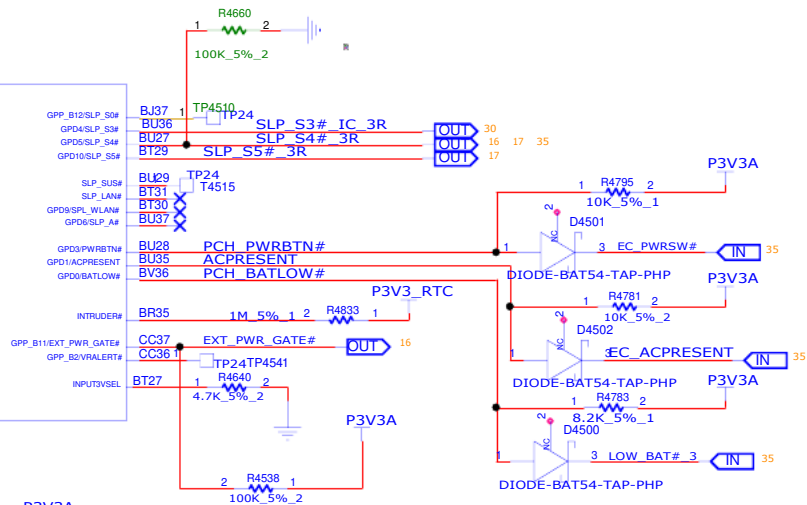
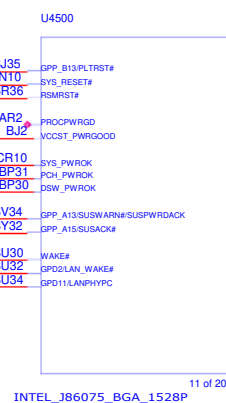
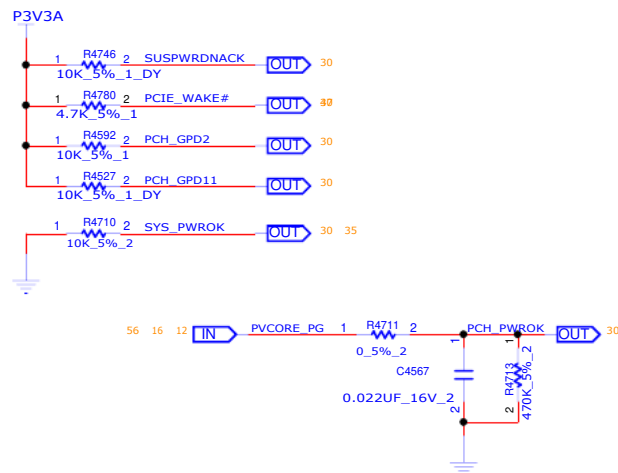
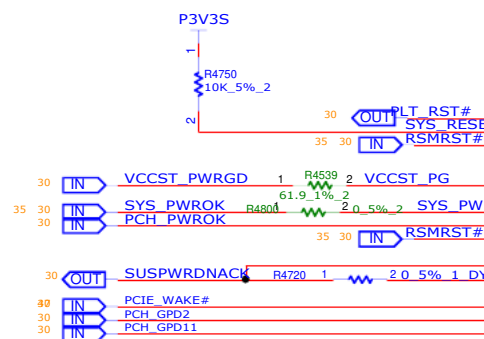
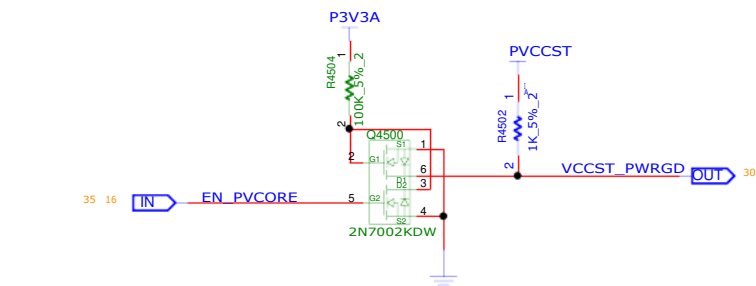


XTAL\_FREQ\_SELECT (GPP\_H21)  
LOW: 38.4/19.2MHZ (DEFAULT)  
HIGH: 24MHZ

INVENTEC

TITLE			
A10 Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV A02
SHEET 29	of 70		

CHANGE by XENG>	DATE 03-Oct-2019
PCB P/N 60xxxxxxxxxx	PCB VER AVER>

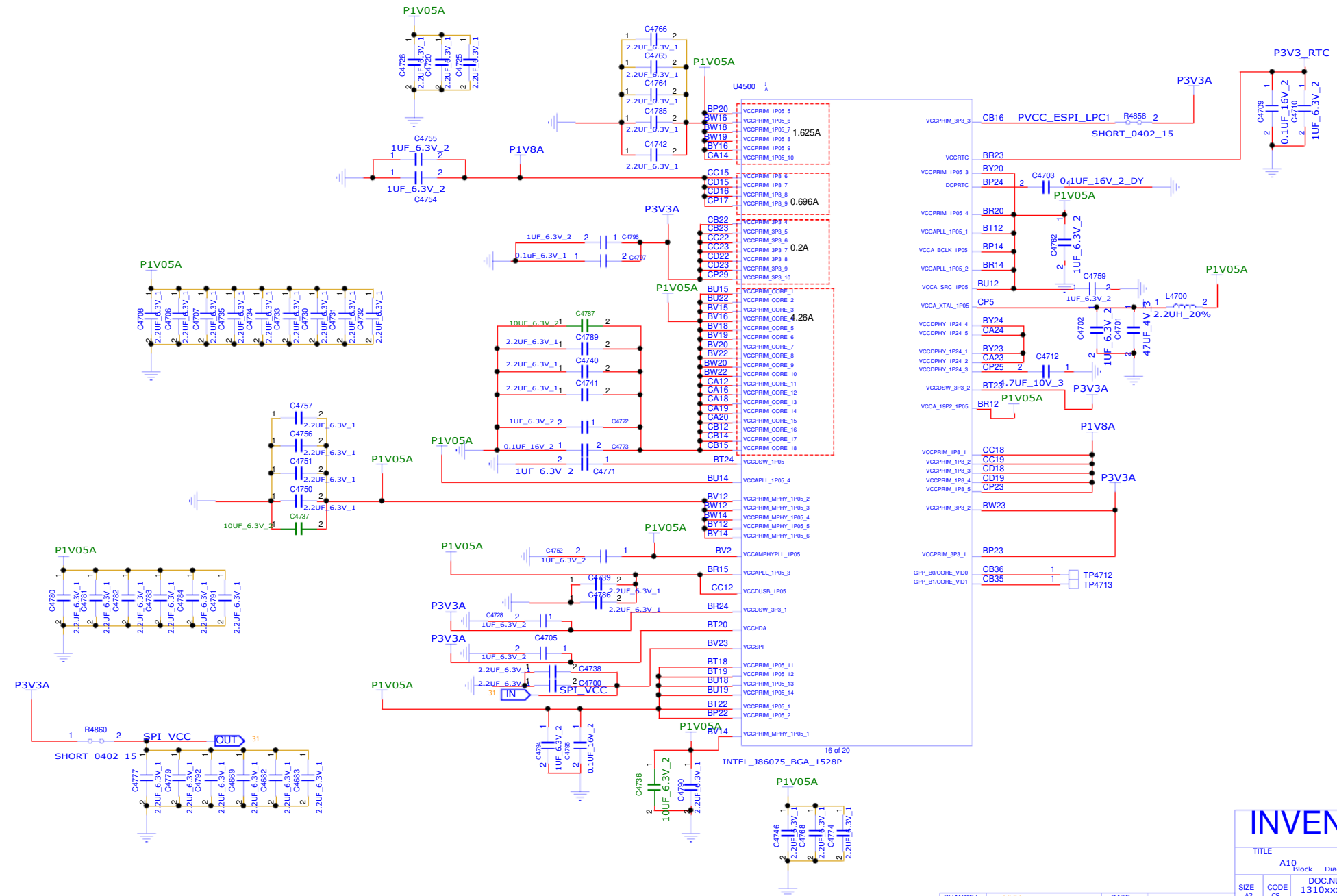


# INVENTEC

TITLE			
A10 Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A02
SHEET 30 of 70			

CHANGE by	XENG>	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	AYEP>

REFERENCE 4700~4949(PCH)



# INVENTEC

TITLE			
A10 Block Diagram			
SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A02
SHEET		of 31	70

CHANGE by	XXX
PCB P/N	60NGxxxxxxx

DATE
PCB VER

A02B9-2019

SIZE A3	CODE CS	1310xxxxx-0-0
SHEET		of 31 70





PVCCGT



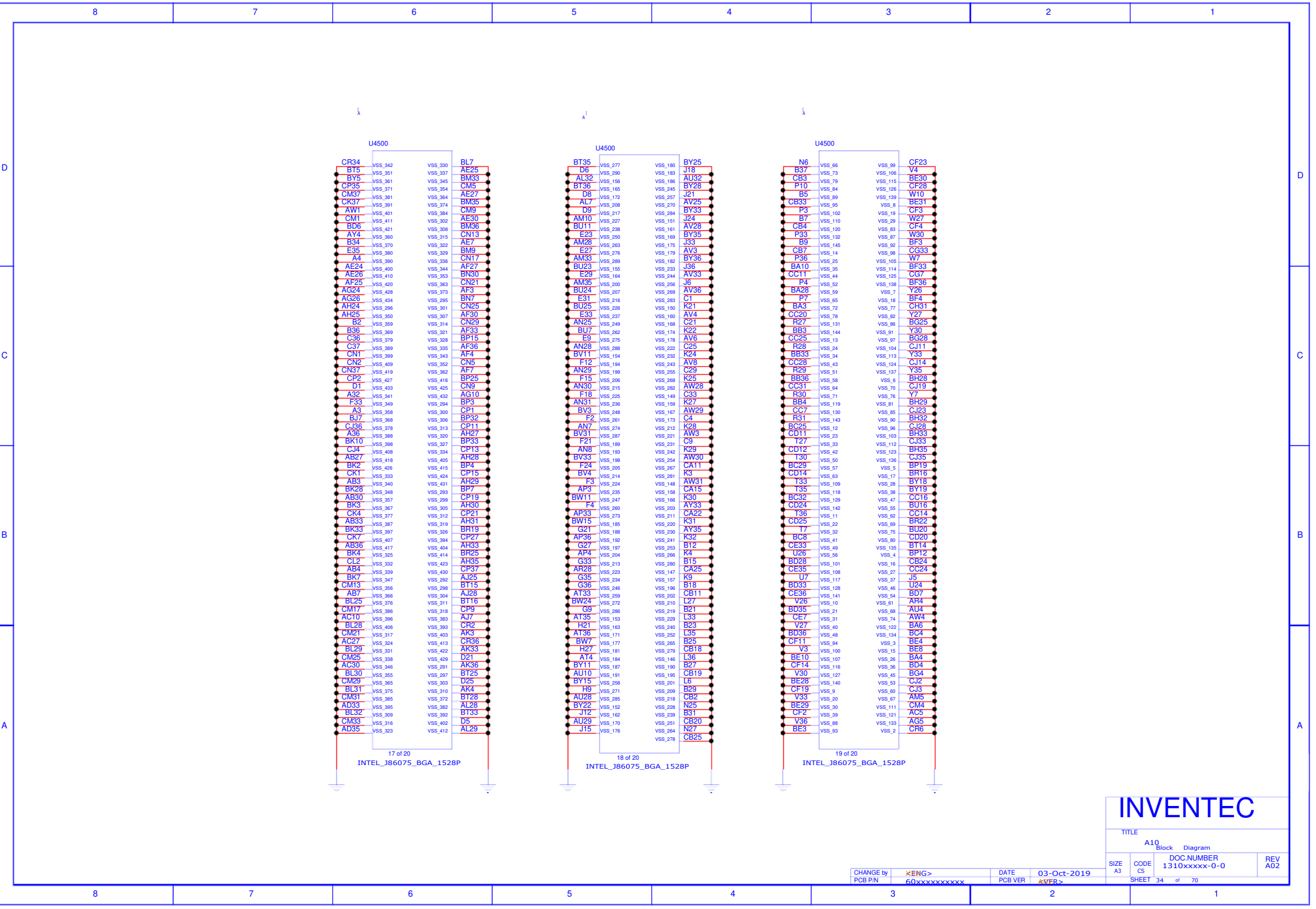
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TITLE

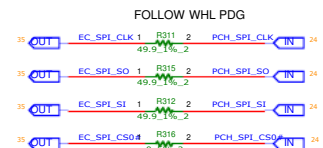
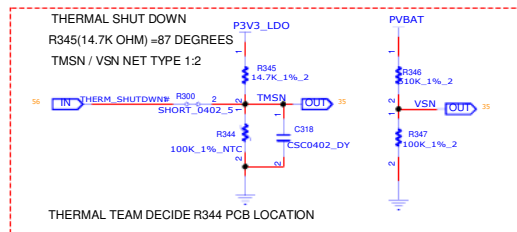
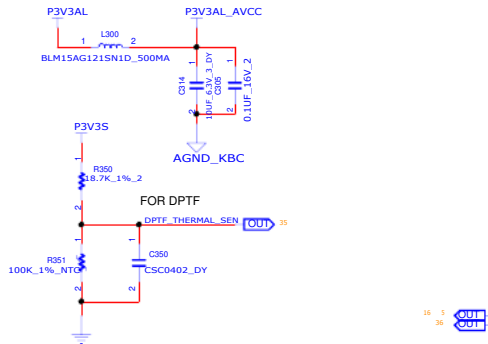
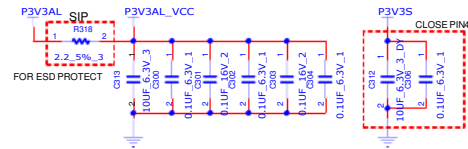
SIZE	CODE	DOC.NUMBER 1310xxxxx-6
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1
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3	2
---	---

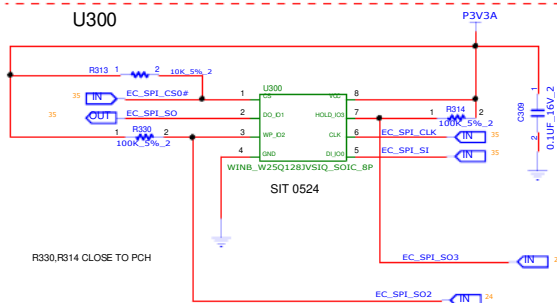


# REFERENCE 300~389(KBC)

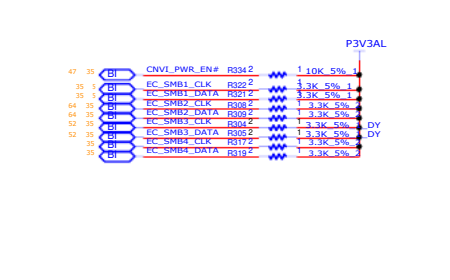
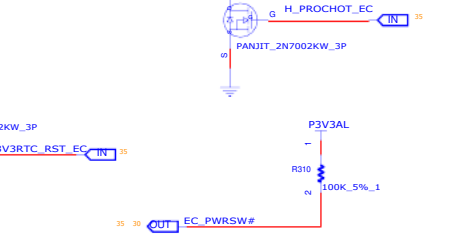
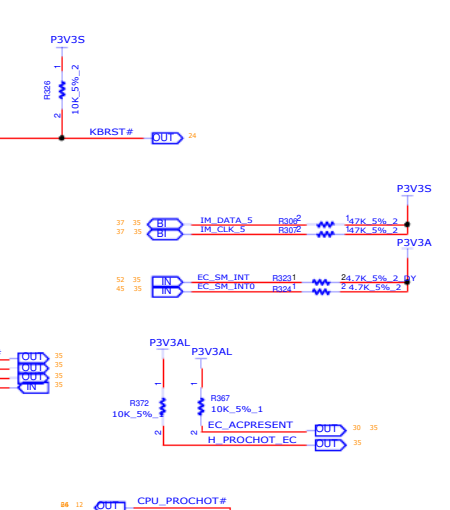
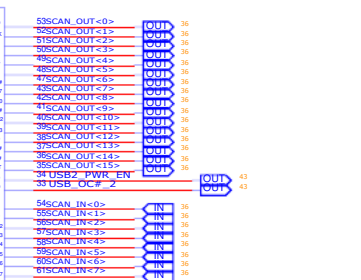
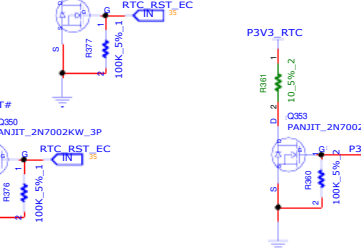
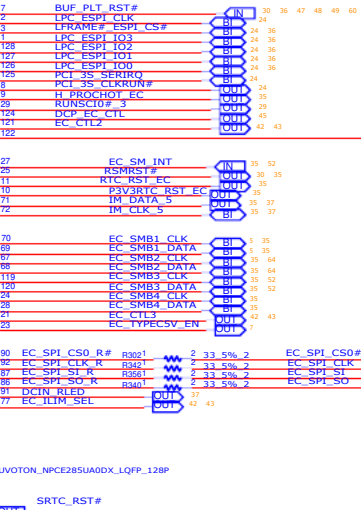
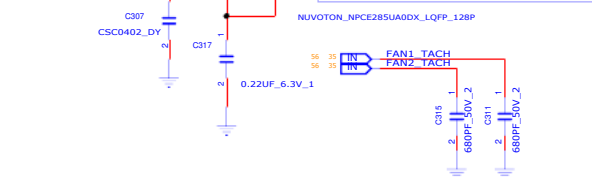
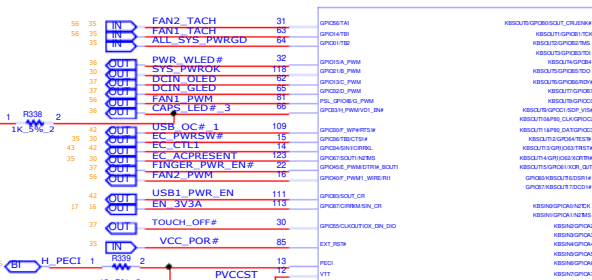
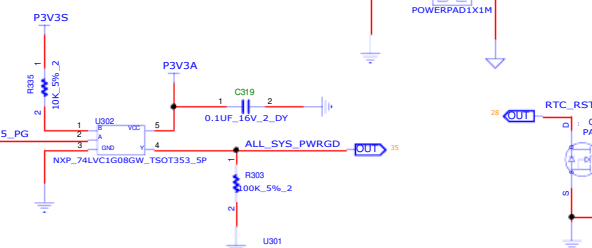
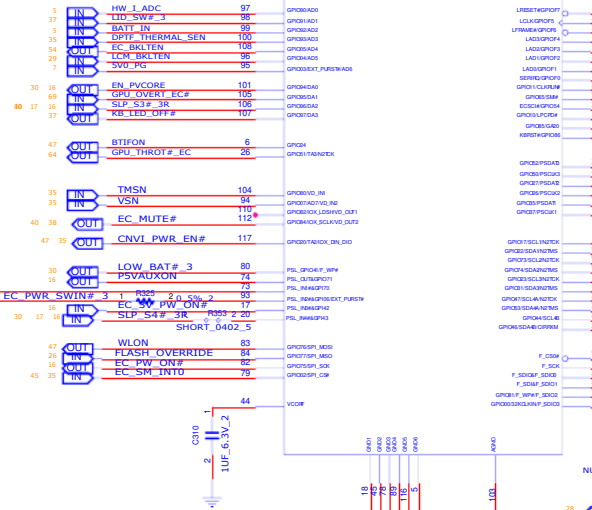


EC_SMB1	EC_SMB2	EC_SMB3	EC_SMB4
BATTERY	GPU	TYPE C	RTK AMP
CHARGE		TYPE C P1	

ALL EC & PCH RESISTOR NEED TO WITHIN 0.5" OF ROM(U300)



R390 FOR INTEL DEBUG

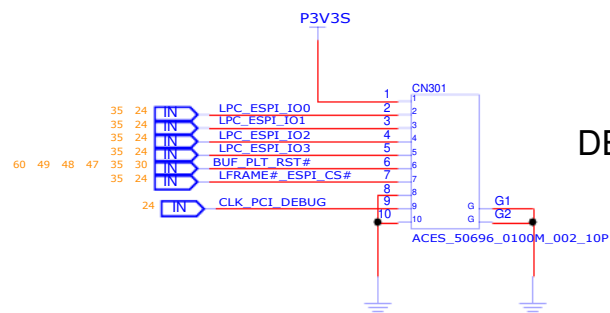


INVENTEC

A

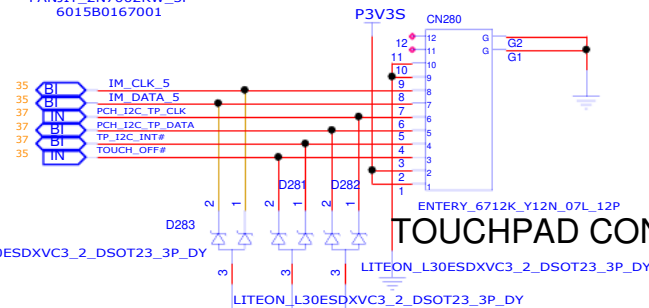
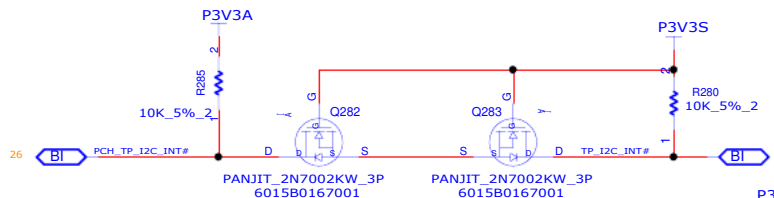
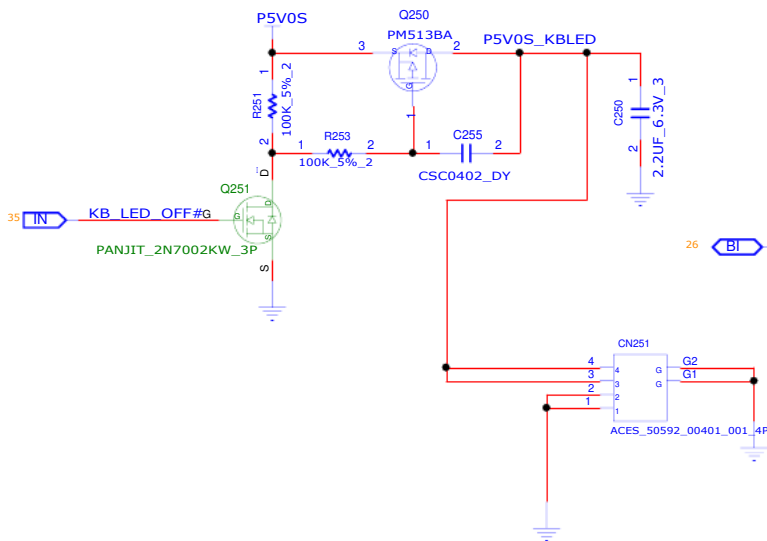
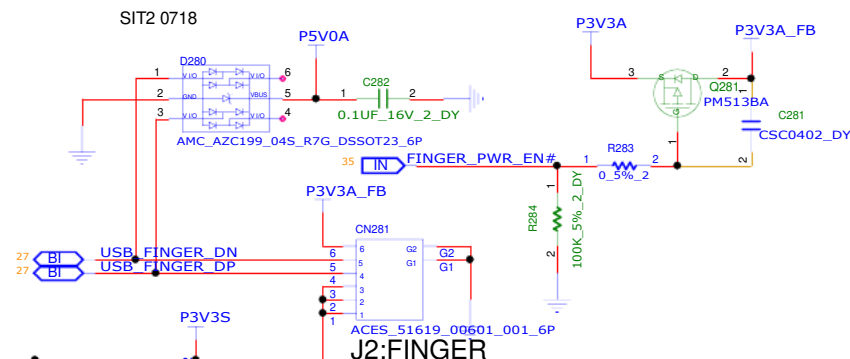
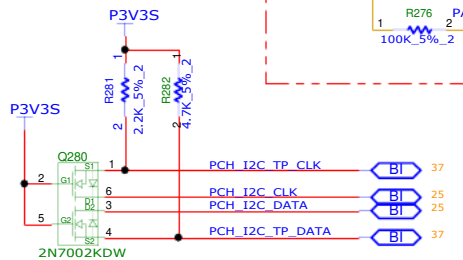
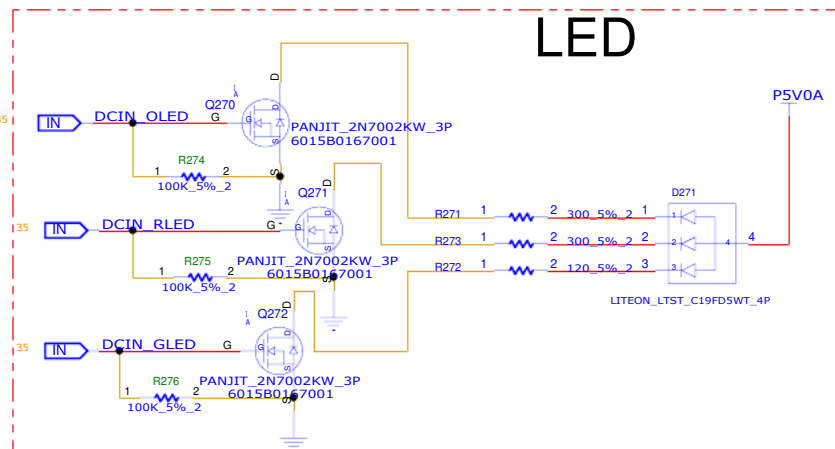
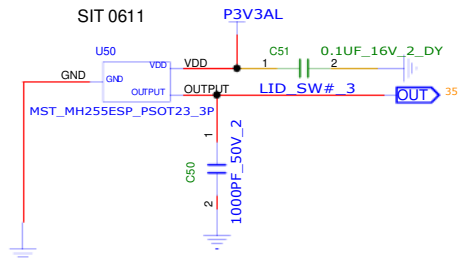


DEBUG CONN



SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A02
SHEET		of 36	70

CHANGE by	XXX	DATE	
PCB P/N	6ENG>XXXXXXXX	PCB VER	A03-Oct-2019



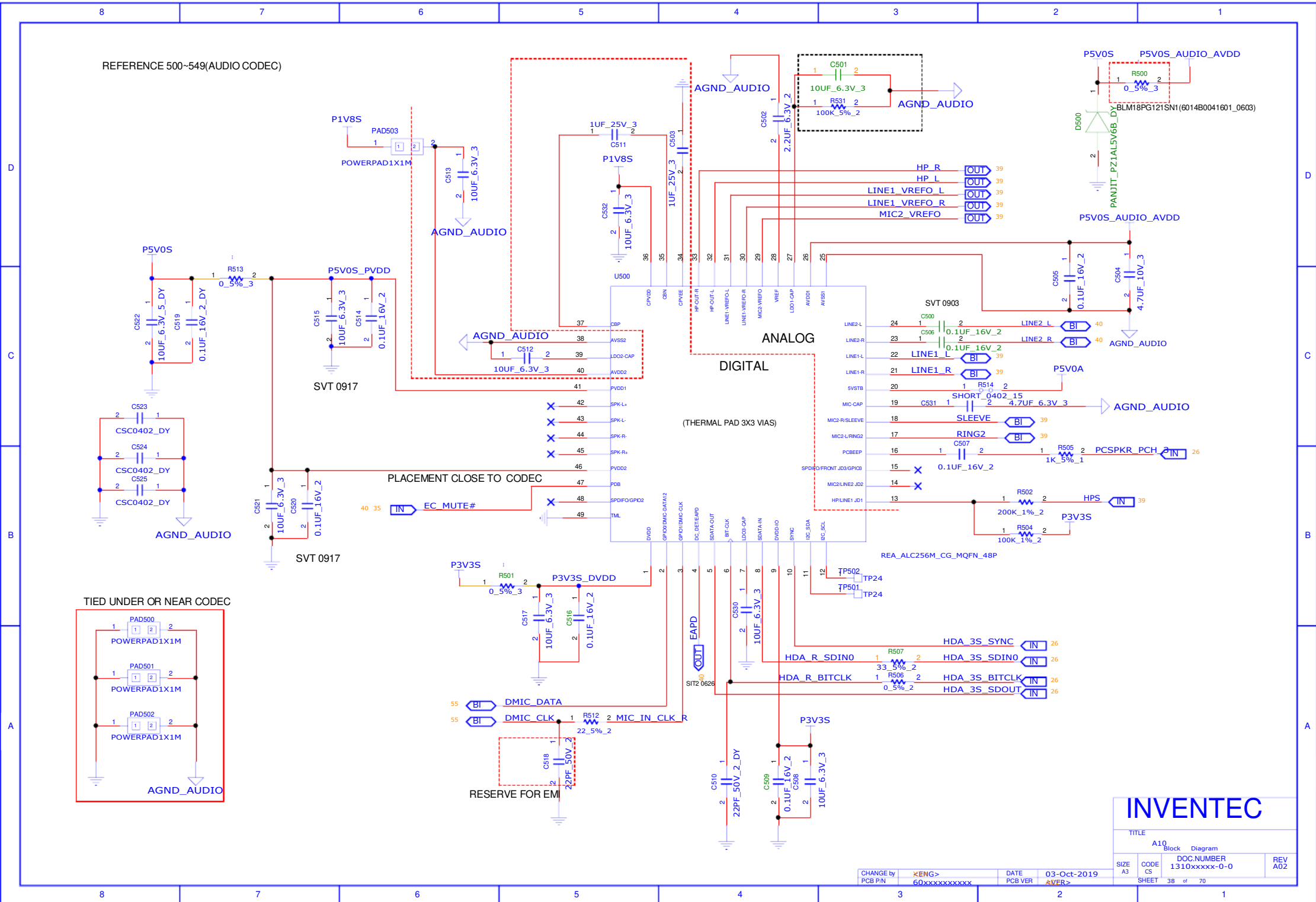
KEYBOARD LED CONN

TOUCHPAD CONN (CLICK PAD)

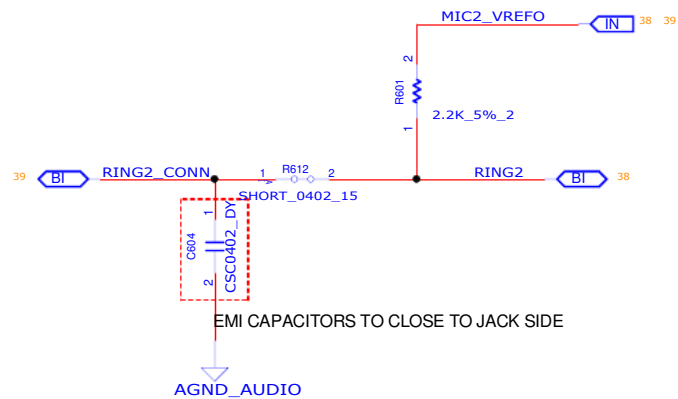
INVENTEC

CHANGE by	XXX	DATE	03-Oct-2019	REV	A02
PCB P/N	60xxxxxxxxxx	PCB VER	A02		

TITLE	A10	Block	Diagram
SIZE	A3	DOC NUMBER	1310xxxx-0-0
CODE	CS	SHEET	37 of 70



# AUDIO JACKS

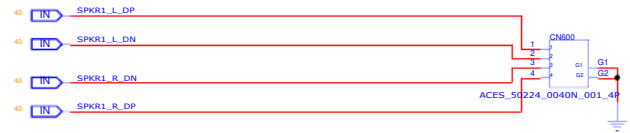


SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0
SHEET		39 of 70

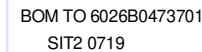
REV  
A02

CHANGE by	XXX	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	A02

	F
	E
	D
	C
	B
	A

[illegible]



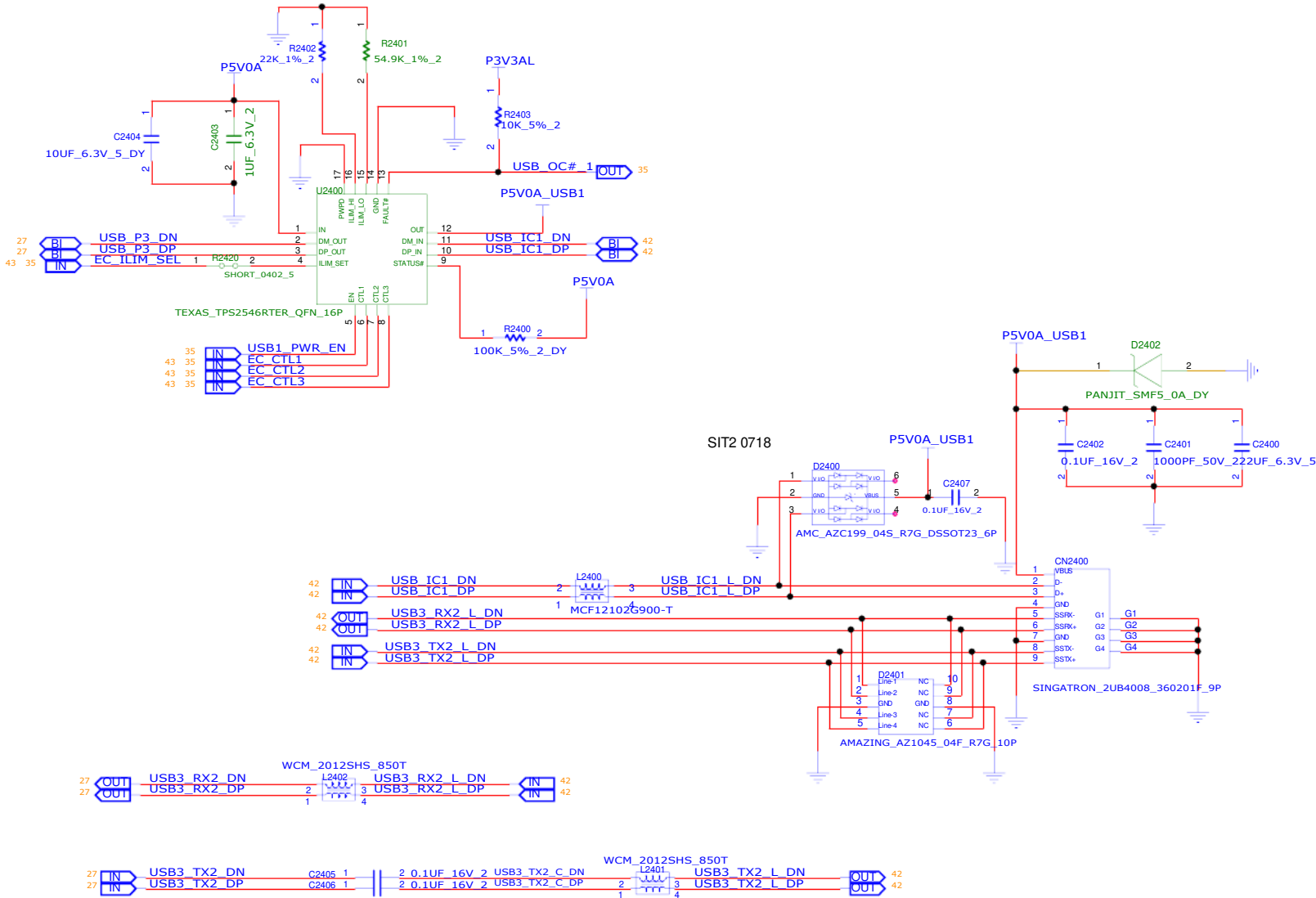


TITLE
A10 CARD READER

SIZE A3	CODE CS	DOC.NUMBER 1310xxxxx-0-0	REV A02
SHEET		41 of 70	

REFERENCE 2400~2450(USB3.0)

# USB 3.0 PORT1

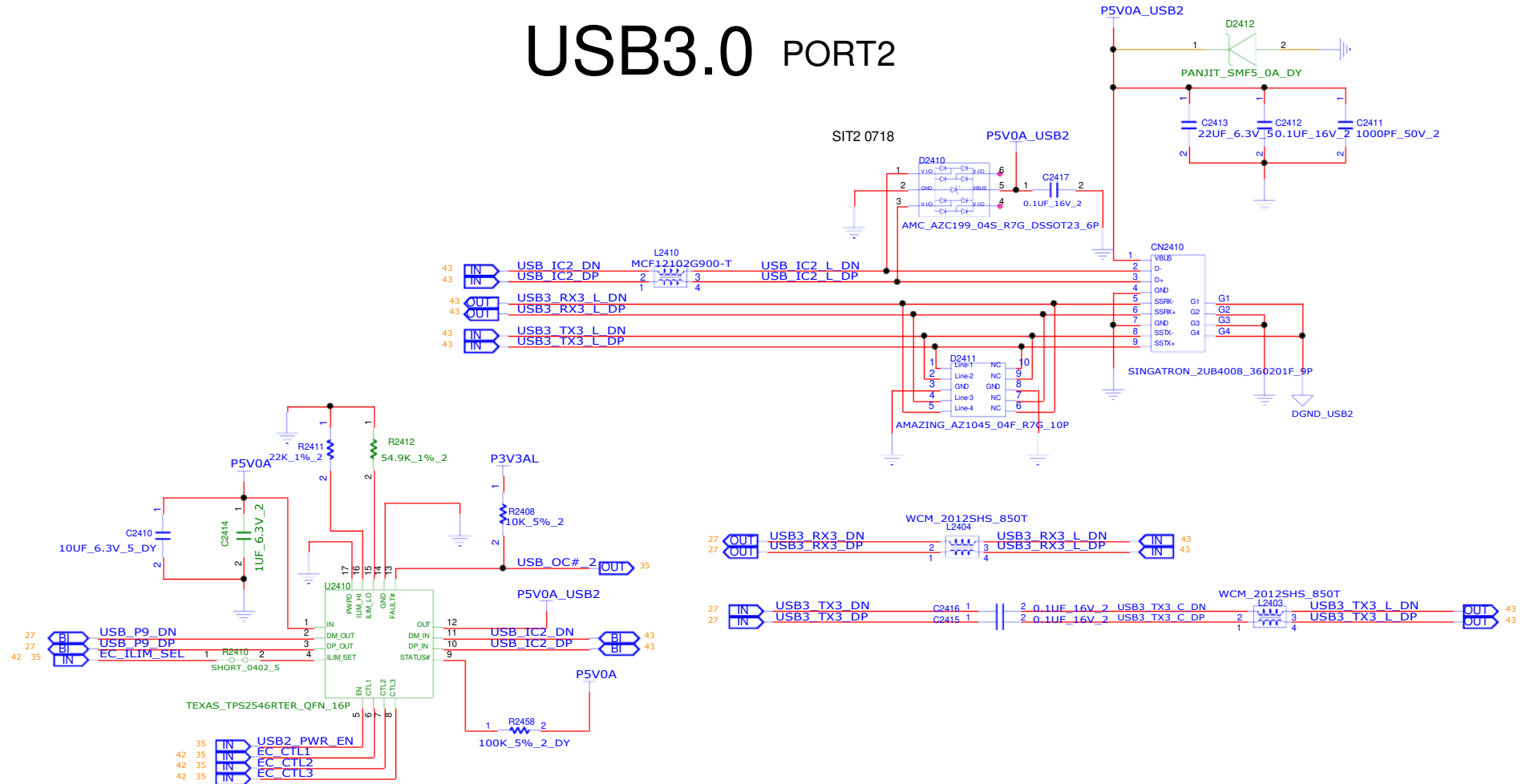


INVENTEC

TITLE			
A10 Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	A02
SHEET		42 of 70	

CHANGE by	XXX	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	A02

# USB3.0 PORT2



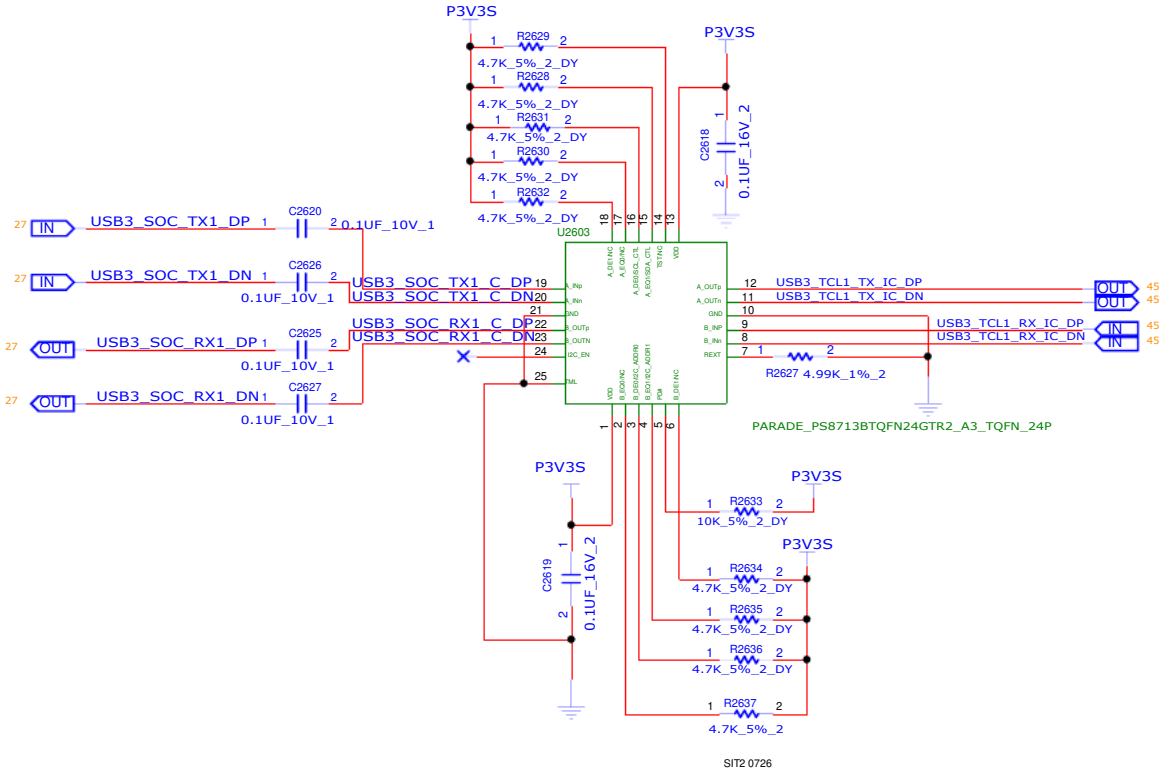
INVENTEC

TITLE			
A10 Block Diagram			
SIZE	CODE	DOC NUMBER	
A3	CS	1310xxxx-0-0	
SHEET	REV		
43 of 70	A02		

CHANGE by	XXX	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	A02

# USB3 REDRIVER 1

REFERENCE 2600~2699(USB RESERVE)



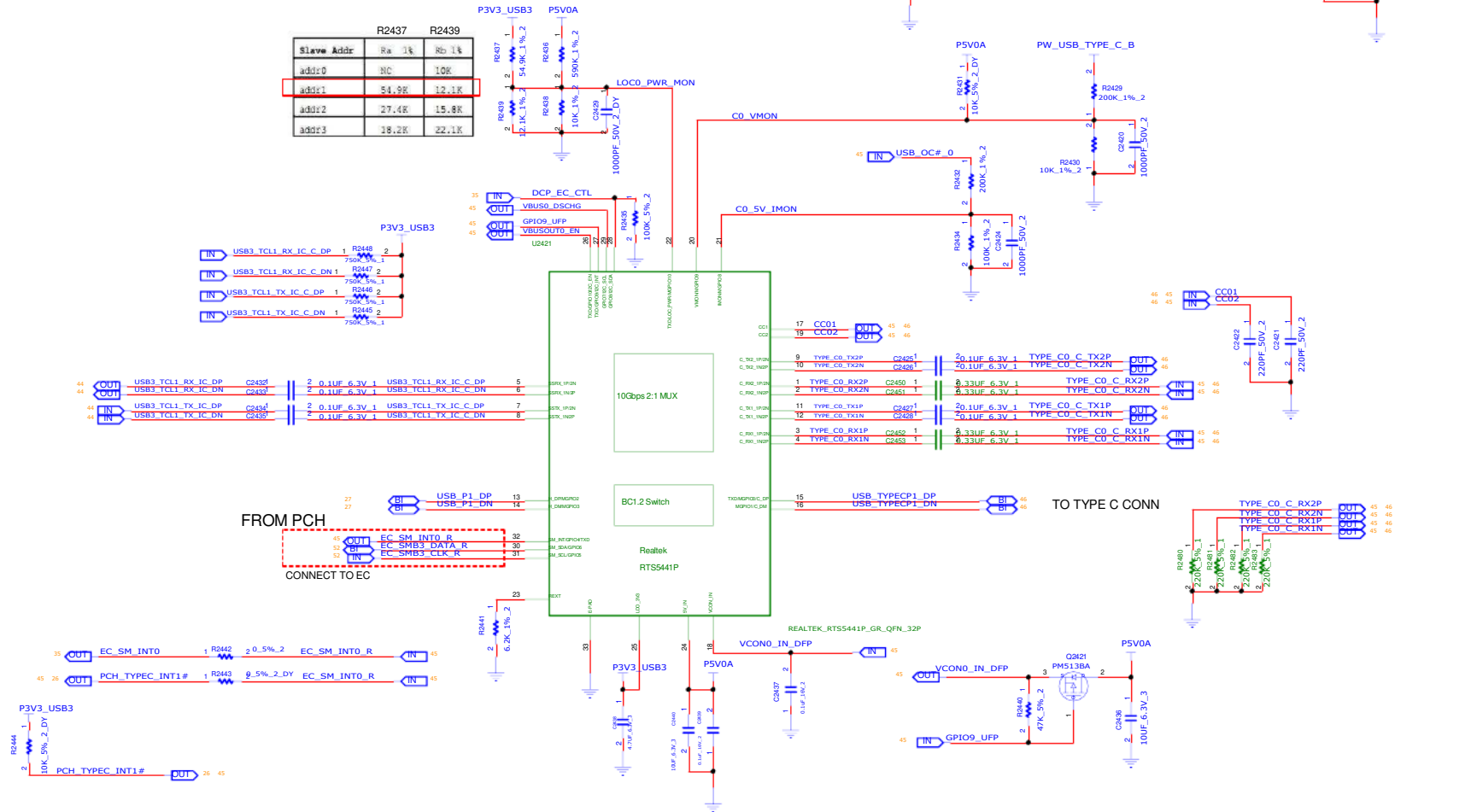
INVENTEC

TITLE  
A10 Block Diagram

SIZE A3  
CODE CS  
DOC NUMBER 1310xxxx-0-0  
SHEET 44 of 70

CHANGE by XXX  
PCB P/N 60xxxxxxxxxx  
DATE 03-Oct-2019  
PCB VER A02

# USB3.1 TYPE C



INVENTEC

A10

TPS5450

SIZE C CODE CS

QCL NUMBER 1310xxxx-0-0

REV A02

CHANGE BY XXXX DATE 03-Oct-2019  
PCB PIN 60xxxxxxx PCB VER AVER>

SHEET 45 20

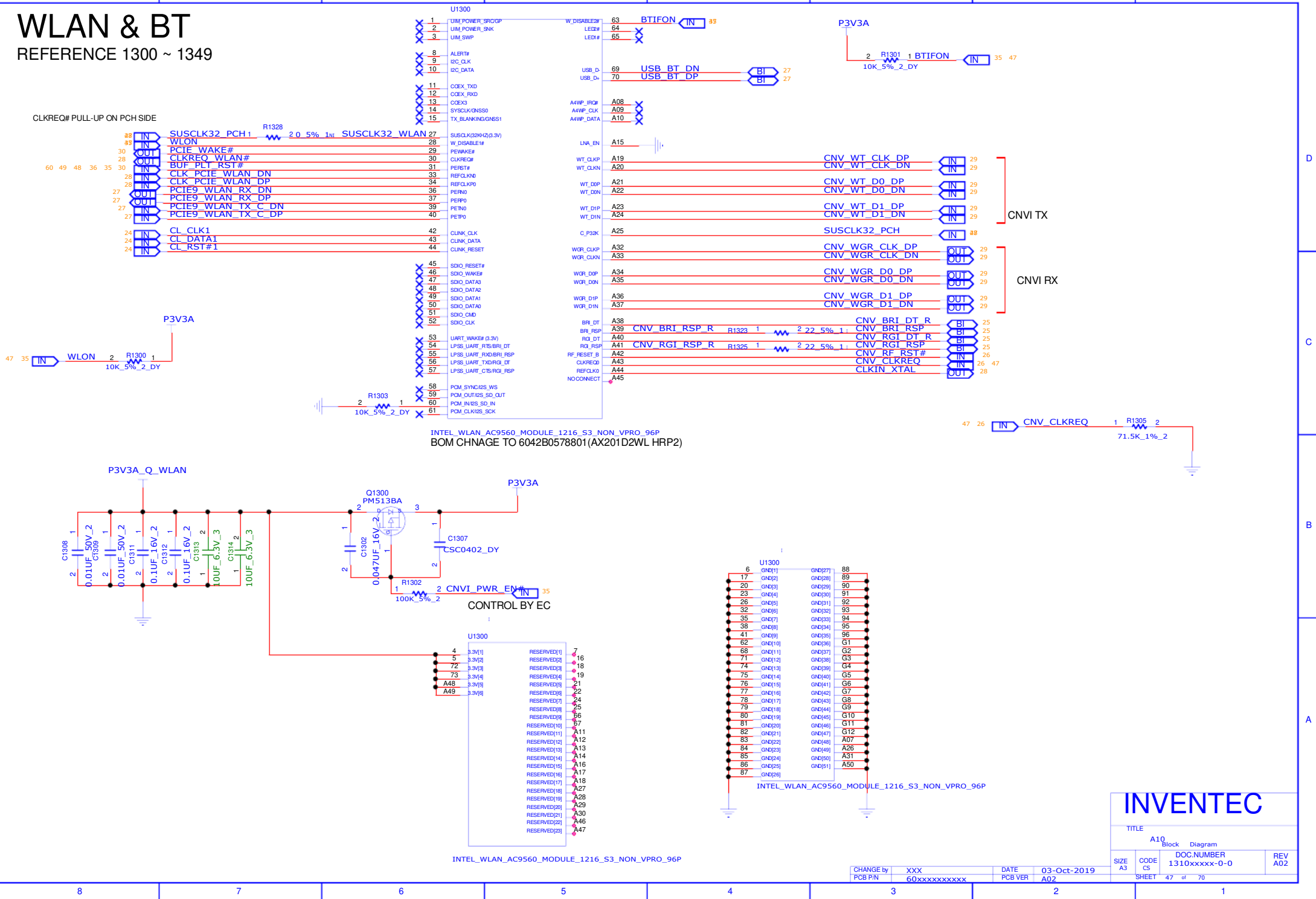
A	B	C	D	E	F
---	---	---	---	---	---

A

# WLAN & BT

## REFERENCE 1300 ~ 1349

CLKREQ# PULL-UP ON PCH SIDE



# INVENTEC

TITLE  
A10 Block Diagram

SIZE A3 CODE CS DOC.NUMBER 1310xxxxx-0-0 REV A02

CHANGE by XXX PCB P/N 60xxxxxxxxxxx DATE 03-Oct-2019 PCB VER A02

SHEET 47 of 70

## D



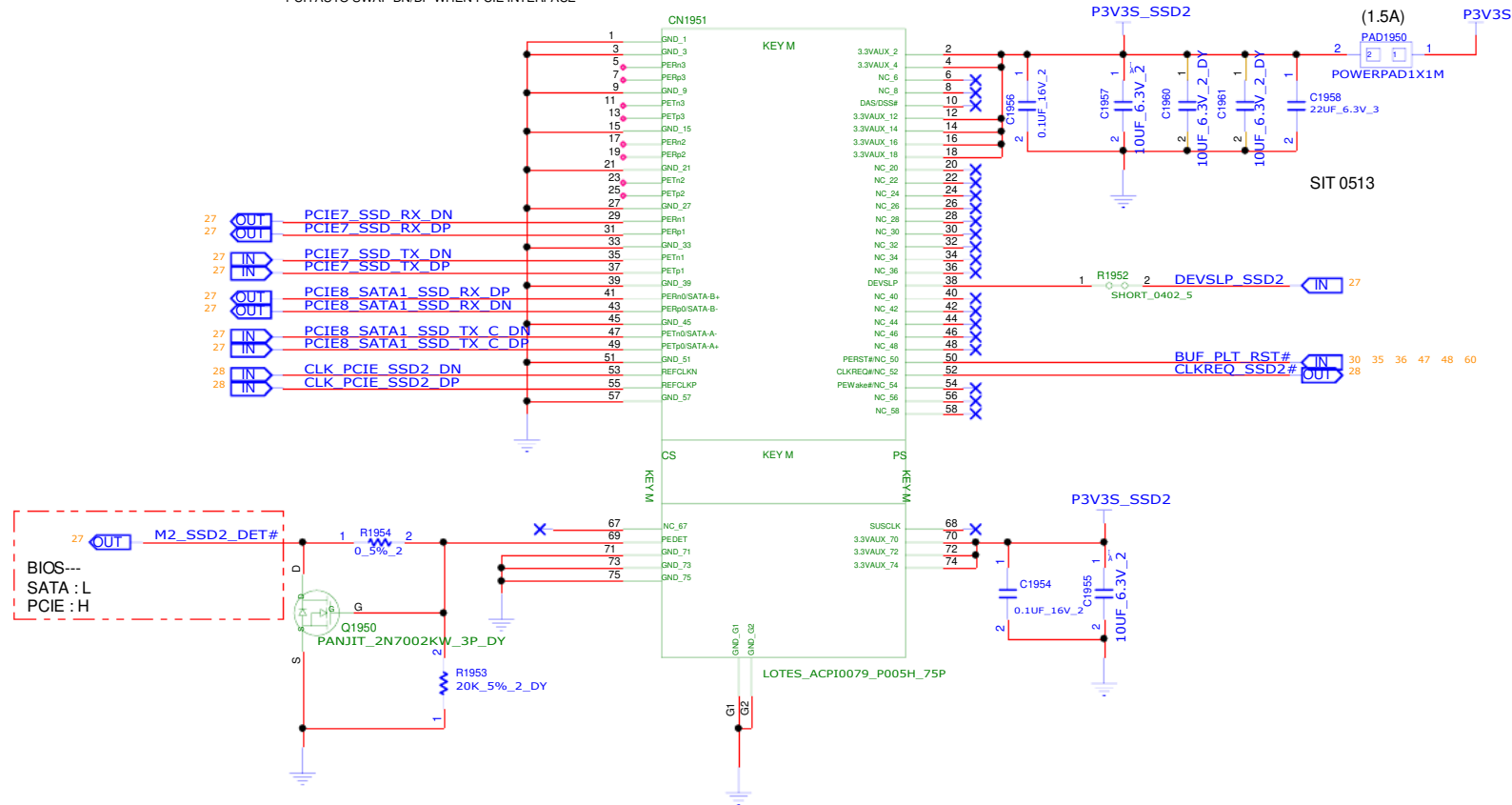
B

A



# NGFF SSD2(PCIE/SATA 2X)

PCH AUTO SWAP DN/DP WHEN PCIE INTERFACE



M.2 CARD USES; SATA SIGNALING (LOW) OR PCIE SIGNALING (HIGH)

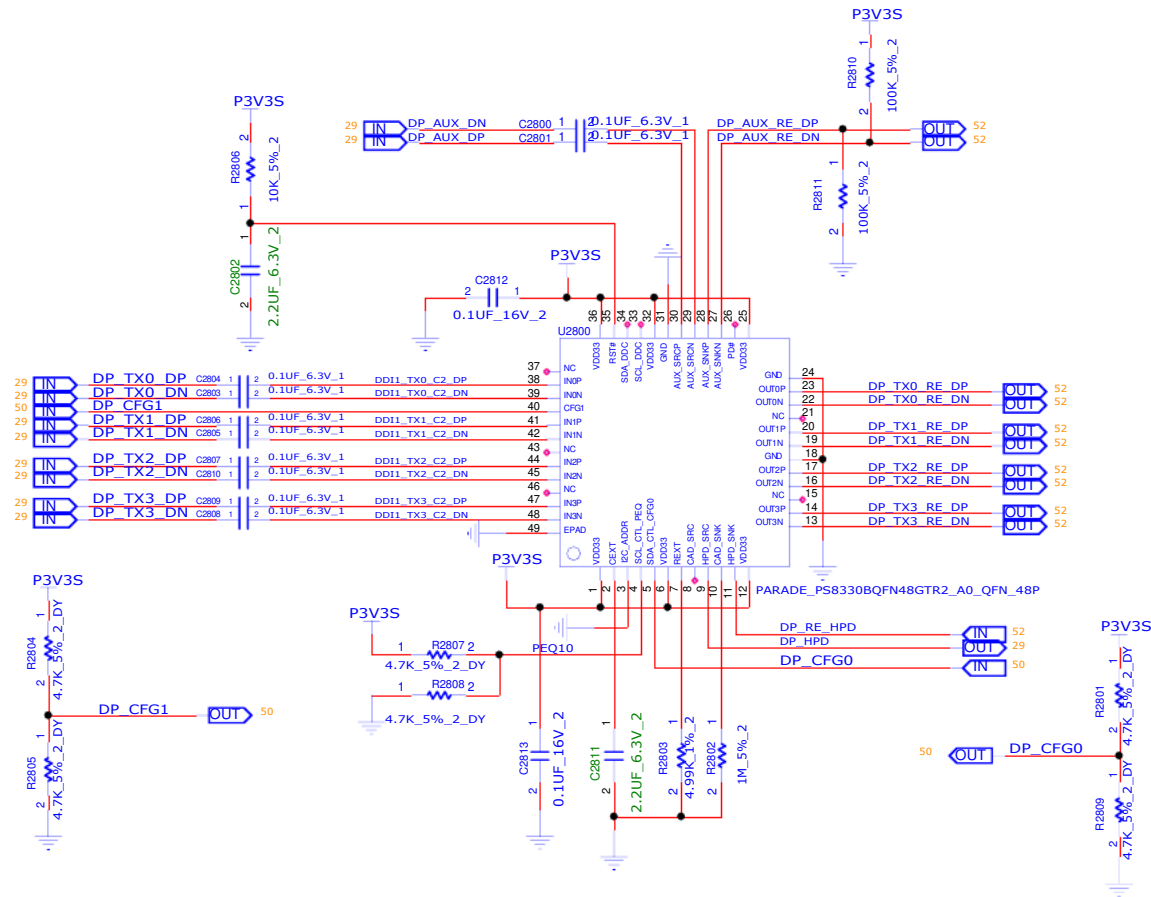
REFERENCE NUMBER:1950~1999

INVENTEC

TITLE			
A10 Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	A02
SHEET		49 of 70	

CHANGE by	XXX	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	A02

# DP REDRIVER

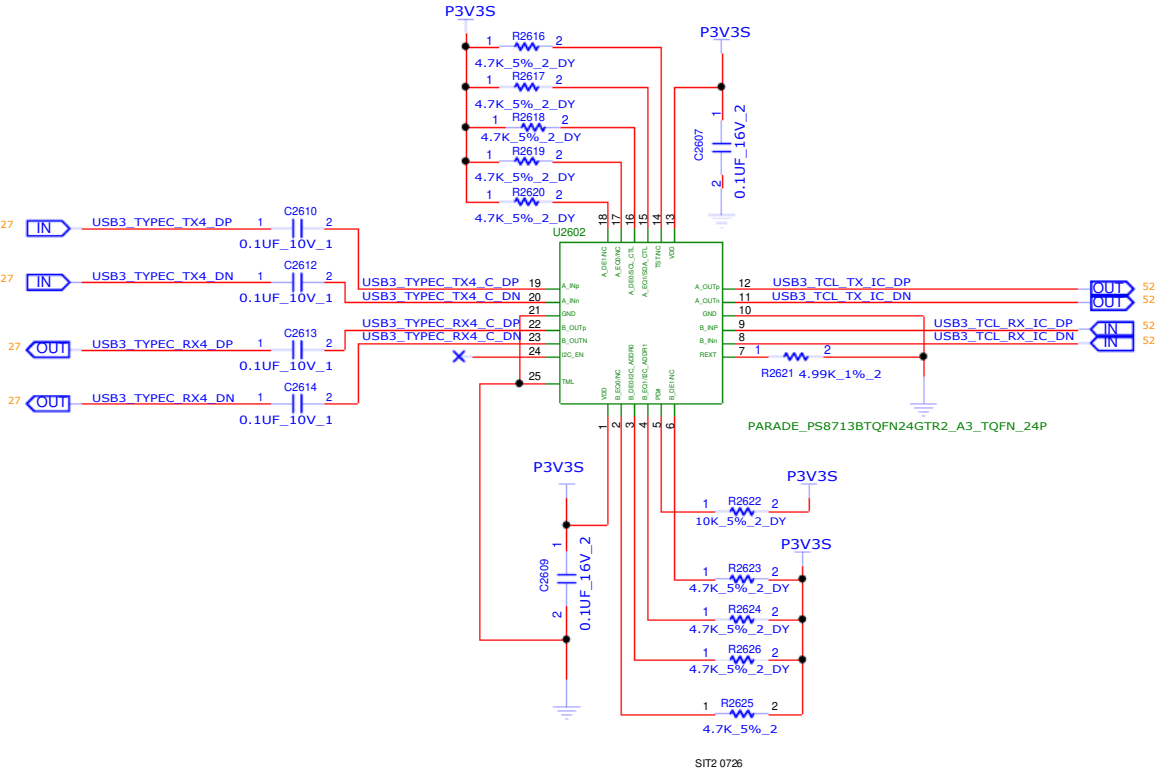


INVENTEC

CHANGE by		XXX	DATE		03-Oct-2019
PCB P/N		60xxxxxxxxxx	PCB VER		A02
SIZE	A3	CODE	CS	DOC NUMBER	1310xxxx-0-0
SHEET	50	of	70	REV	A02

# USB3 REDRIVER

REFERENCE 2600~2699(USB RESERVE)

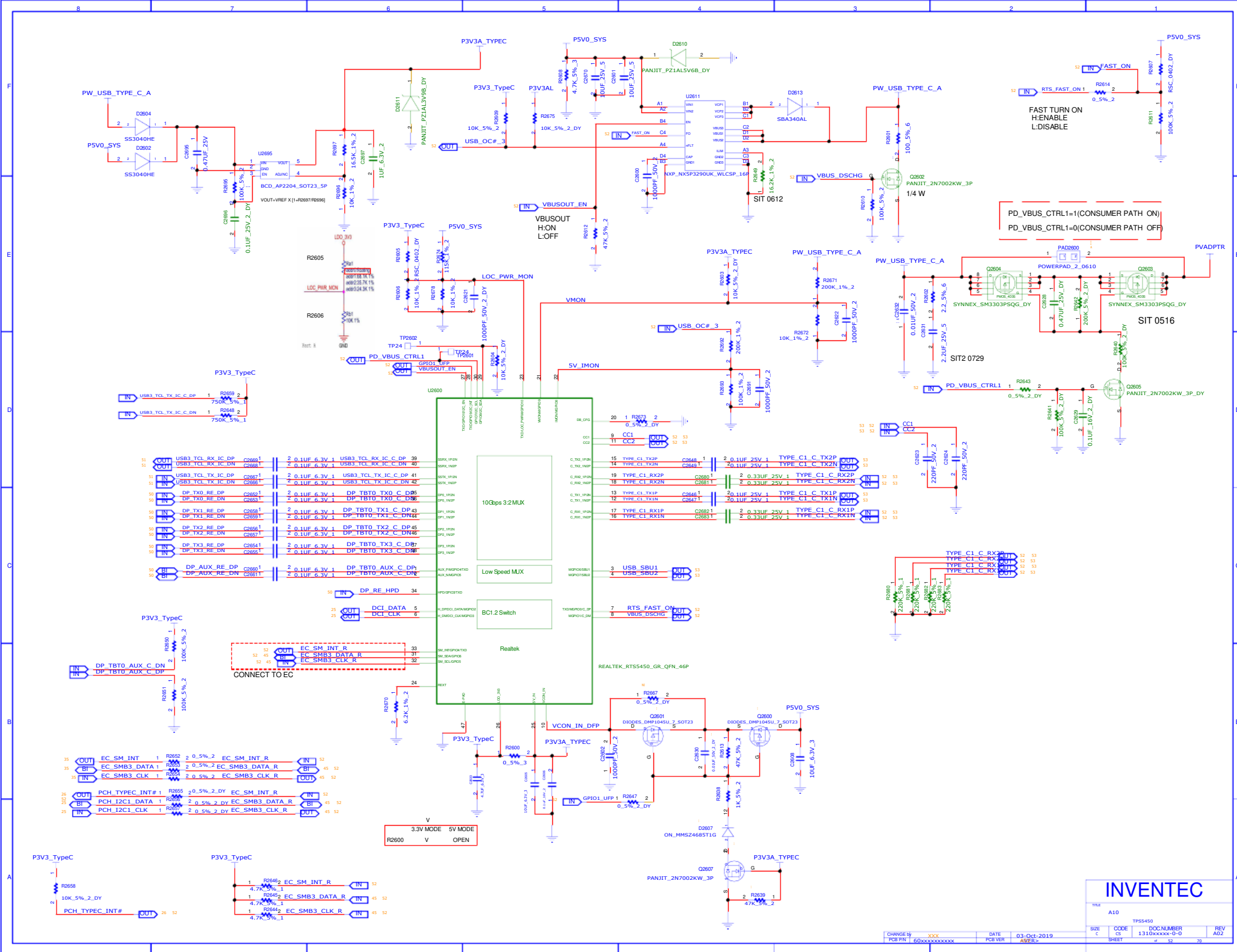


INVENTEC

TITLE  
A10 Block Diagram

SIZE A3	CODE CS	DOC NUMBER 1310xxxx-0-0	REV A02
SHEET 51	of 70		

CHANGE by PCB P/N	XXX 60xxxxxxxxxx	DATE PCB VER	03-Oct-2019 A02
----------------------	---------------------	-----------------	--------------------

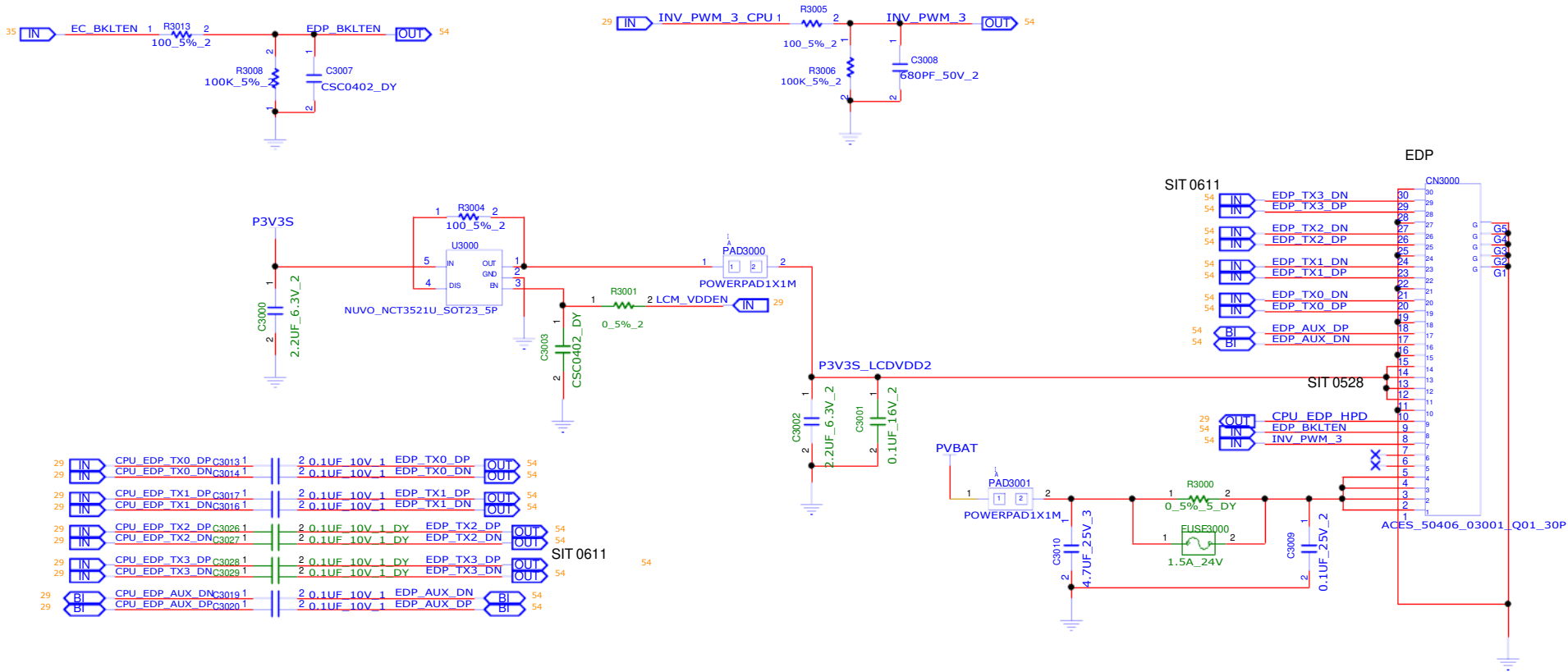


INVENTEC			
TITLE			
A10			
TPS4540			
DOC NUMBER			
1310xxxx-0-0			
REV			
A02			
SHEET			
52			
20			

CHANGE BY: XXXX  
PCB PIN: 60xxxxxxx  
DATE: 03-Oct-2019  
PCB VER: A10ER>



# EDP CONN

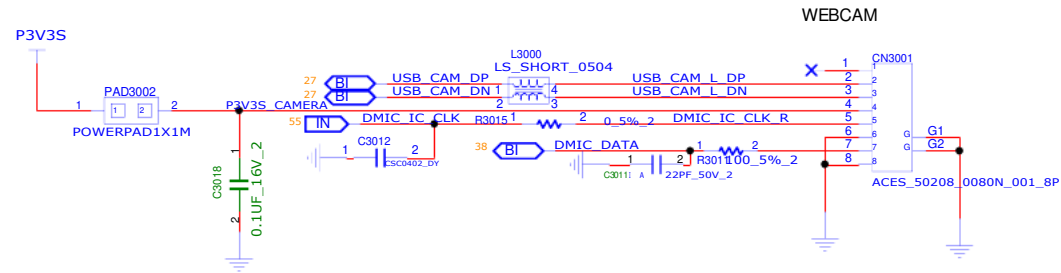
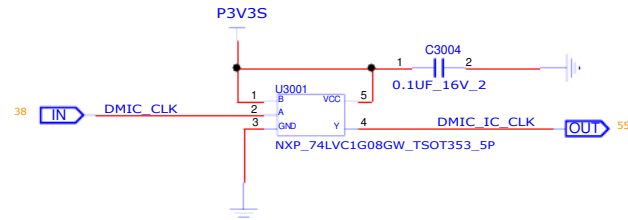


INVENTEC

TITLE			
A10 Block Diagram			
SIZE	CODE	DOC NUMBER	REV
A3	CS	1310xxxx-0-0	A02
SHEET	54	of 70	

CHANGE by	XXX	DATE	03-Oct-2019
PCB P/N	60xxxxxxxxxx	PCB VER	A02

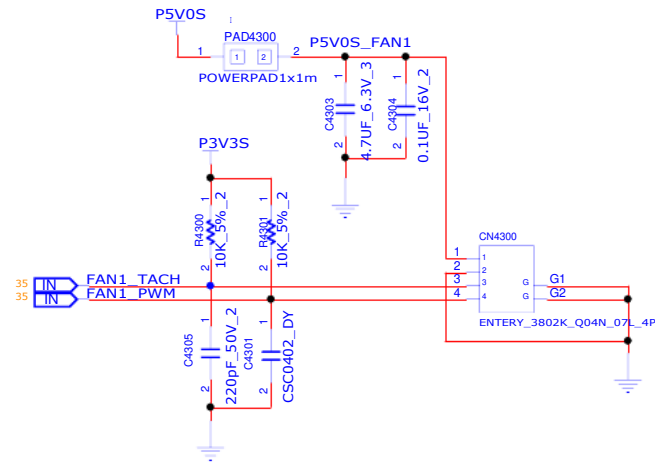
## WEBCAM



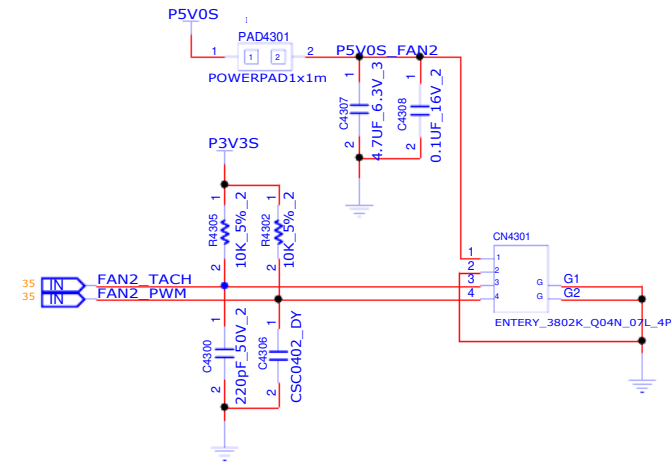
## INVENTEC

CHANGE by	XXX	DATE	03-Oct-2019	SIZE	CODE	1310xxxxx-0-0	A02
PCB P/N	60xxxxxxxxxx	PCB VER	A02	A3	CS		
				SHEET	55	of 70	

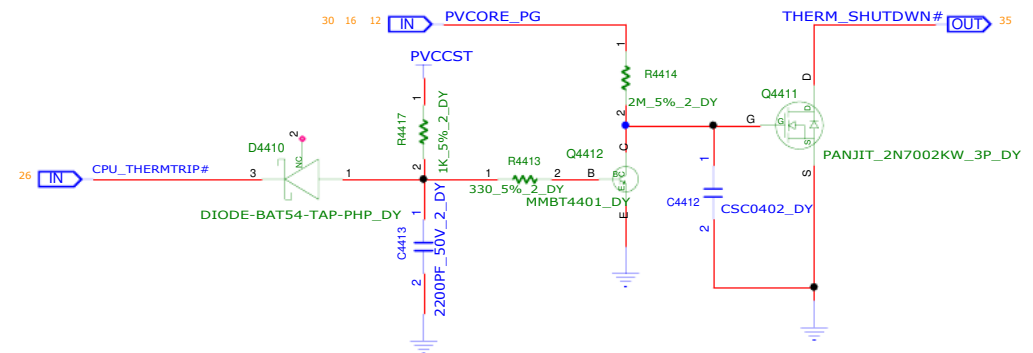
REFERENCE 4300~4349(FAN)  
REFERENCE 4411~4449(THERMAL )



FAN1 CN CPU



# FAN2 CN CPU



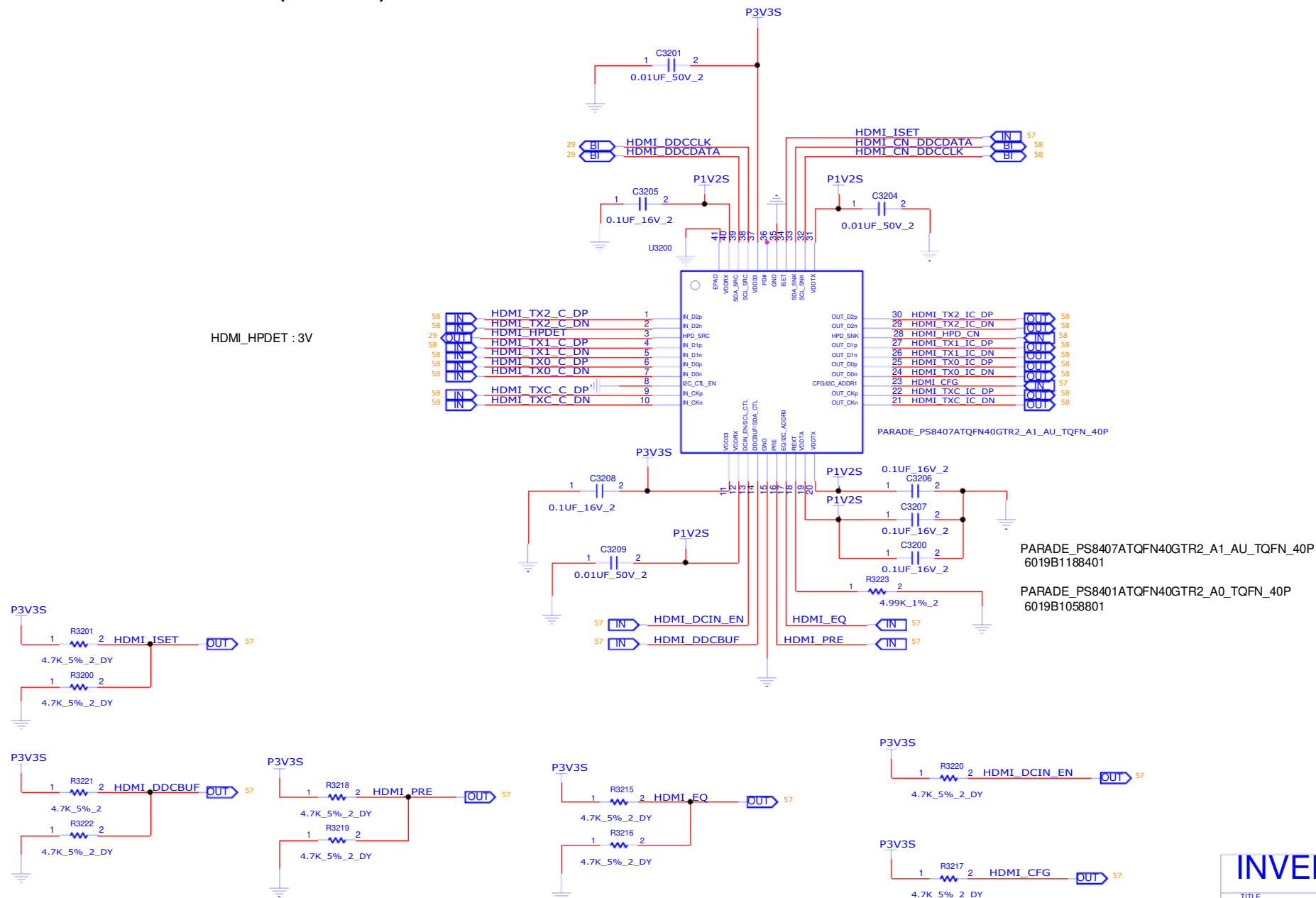
REFERENCE NUMBER:4411~4449

# INVENTEC

						TITLE			
						A10 Block Diagram			
CHANGE by		XXX	DATE			SIZE	CODE	DOC NUMBER	REV
PCB P/N		XXXXXX	PCB VER	A03-Oct-2019		A3	CS	1310xxxxx-0-0	A02
						SHEET of 56 70			

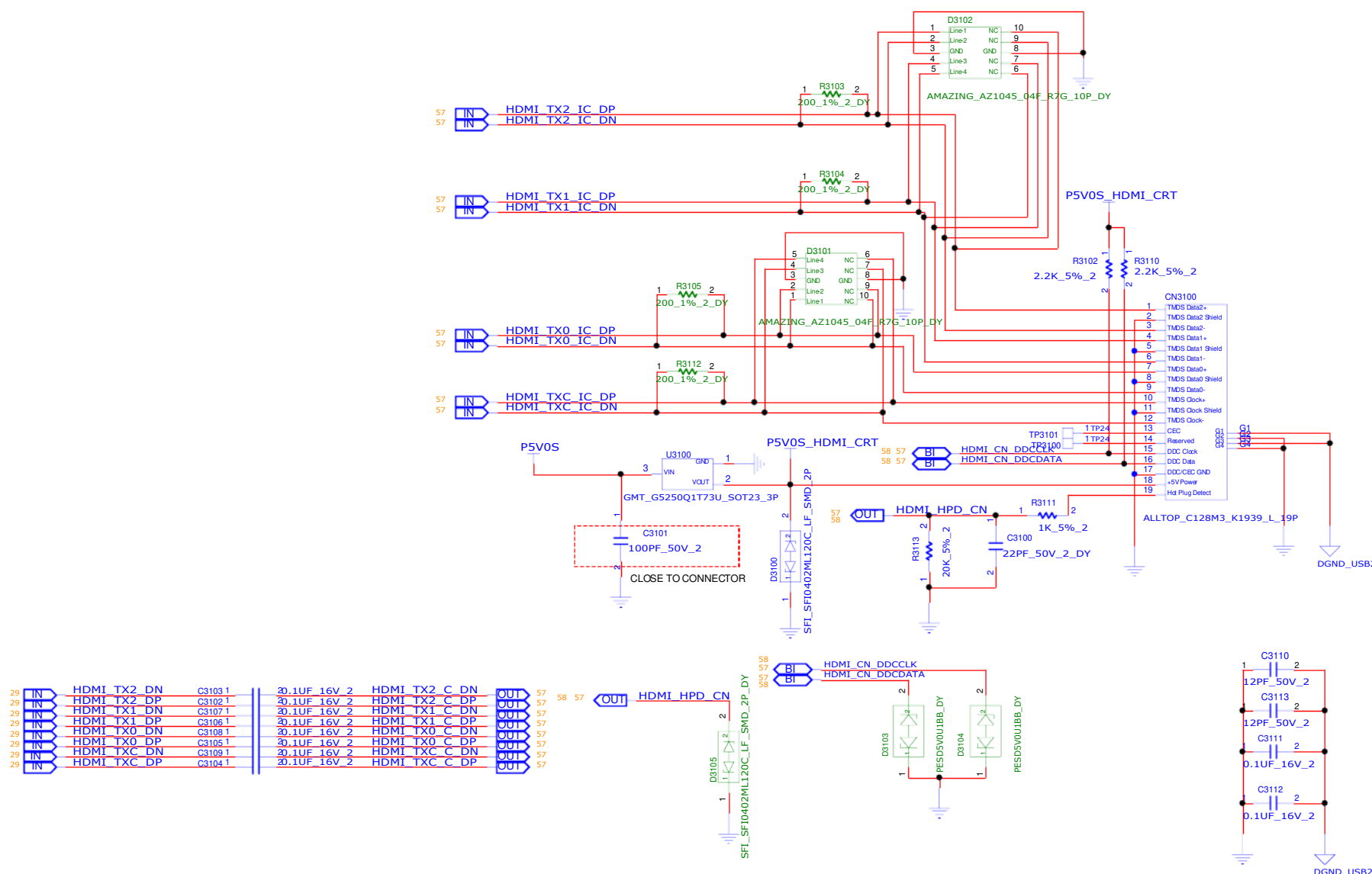


## HDMI REPEATER (4K2K)



INVENTEC

TITLE  
A10 Block DiagramSIZE A3  
CODE CS  
SHEET 57 of 70DOC NUMBER  
1310xxxx-0-0REV  
A02CHANGE by XXX  
PCB P/N 60xxxxxxxxxx  
DATE 03-Oct-2019  
PCB VER A02



29	IN	HDMI TX2 DN	C3103.1	20.1UF 16V 2	HDMI TX2 C DN	OUT	57
29	IN	HDMI TX2 DP	C3102.1	20.1UF 16V 2	HDMI TX2 C DP	OUT	57
29	IN	HDMI TX1 DN	C3107.1	20.1UF 16V 2	HDMI TX1 C DN	OUT	57
29	IN	HDMI TX1 DP	C3106.1	20.1UF 16V 2	HDMI TX1 C DP	OUT	57
29	IN	HDMI TX0 DN	C3108.1	20.1UF 16V 2	HDMI TX0 C DN	OUT	57
29	IN	HDMI TX0 DP	C3105.1	20.1UF 16V 2	HDMI TX0 C DP	OUT	57
29	IN	HDMI TXC DN	C3109.1	20.1UF 16V 2	HDMI TXC C DN	OUT	57
29	IN	HDMI TXC DP	C3104.1	20.1UF 16V 2	HDMI TXC C DP	OUT	57

INVENTEC

TITLE			
A10 Block Diagram			
SIZE A3	CODE CS	DOC NUMBER 1310xxxxx-0-0	REV A02
CHANGE by PCB P/N		DATE PCB VER	03-Oct-2019 A02
XXX 60xxxxxxxxxx		SHEET 58 of 70	

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NOTES:  
1. HSF Property: Comply iSupplier system HSF property attribute up-to-date value.

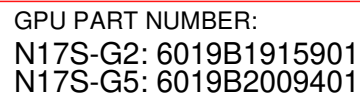
# N17S-G2/G5

## GDDR5 23X23

2019.12.11

03-Oct-2019		
DATE	CHANGE NO.	REV

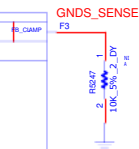
Chen Sheng Huang Vens			Shu Vvi			INVENTEC		
DESIGN / DRAWER	XXX	DATE	03-Oct-2019	TITLE	A10			
CHECK				SIZE	C0	DOC NUMBER	1310xxxx-0-0	REV A02
APPROVAL			A01					
FILE NAME								
PCB PIN	06R05xxxxxxx	PCB VER	A02	SHEET	of 99	25		



IC: RGA\_NV080\_2300\_2300\_195  
U5000

65	BI	FBA_D<0>	E18	FBA_D0
65	BI	FBA_D<1>	F18	FBA_D1
65	BI	FBA_D<2>	F18	FBA_D2
65	BI	FBA_D<3>	F17	FBA_D3
65	BI	FBA_D<4>	U0	FBA_D4
65	BI	FBA_D<5>	U0	FBA_D5
65	BI	FBA_D<6>	F21	FBA_D6
65	BI	FBA_D<7>	F21	FBA_D7
65	BI	FBA_D<8>	E18	FBA_D8
65	BI	FBA_D<9>	D18	FBA_D9
65	BI	FBA_D<10>	F18	FBA_D10
65	BI	FBA_D<11>	F18	FBA_D11
65	BI	FBA_D<12>	C18	FBA_D12
65	BI	FBA_D<13>	B18	FBA_D13
65	BI	FBA_D<14>	E19	FBA_D14
65	BI	FBA_D<15>	D18	FBA_D15
65	BI	FBA_D<16>	F18	FBA_D16
65	BI	FBA_D<17>	C18	FBA_D17
65	BI	FBA_D<18>	A18	FBA_D18
65	BI	FBA_D<19>	B18	FBA_D19
65	BI	FBA_D<20>	B18	FBA_D20
65	BI	FBA_D<21>	A18	FBA_D21
65	BI	FBA_D<22>	A18	FBA_D22
65	BI	FBA_D<23>	C18	FBA_D23
65	BI	FBA_D<24>	C18	FBA_D24
65	BI	FBA_D<25>	C18	FBA_D25
65	BI	FBA_D<26>	A20	FBA_D26
65	BI	FBA_D<27>	A20	FBA_D27
65	BI	FBA_D<28>	A21	FBA_D28
65	BI	FBA_D<29>	C18	FBA_D29
65	BI	FBA_D<30>	C18	FBA_D30
65	BI	FBA_D<31>	C18	FBA_D31
65	BI	FBA_D<32>	B18	FBA_D32
65	BI	FBA_D<33>	B18	FBA_D33
65	BI	FBA_D<34>	B18	FBA_D34
65	BI	FBA_D<35>	B18	FBA_D35
65	BI	FBA_D<36>	N20	FBA_D36
65	BI	FBA_D<37>	N20	FBA_D37
65	BI	FBA_D<38>	N20	FBA_D38
65	BI	FBA_D<39>	V23	FBA_D39
65	BI	FBA_D<40>	V23	FBA_D40
65	BI	FBA_D<41>	V22	FBA_D41
65	BI	FBA_D<42>	V22	FBA_D42
65	BI	FBA_D<43>	U22	FBA_D43
65	BI	FBA_D<44>	V24	FBA_D44
65	BI	FBA_D<45>	A24	FBA_D45
65	BI	FBA_D<46>	V22	FBA_D46
65	BI	FBA_D<47>	A20	FBA_D47
65	BI	FBA_D<48>	A20	FBA_D48
65	BI	FBA_D<49>	A20	FBA_D49
65	BI	FBA_D<50>	A20	FBA_D50
65	BI	FBA_D<51>	A20	FBA_D51
65	BI	FBA_D<52>	A20	FBA_D52
65	BI	FBA_D<53>	A20	FBA_D53
65	BI	FBA_D<54>	V28	FBA_D54
65	BI	FBA_D<55>	V28	FBA_D55
65	BI	FBA_D<56>	F18	FBA_D56
65	BI	FBA_D<57>	F18	FBA_D57
65	BI	FBA_D<58>	N20	FBA_D58
65	BI	FBA_D<59>	N20	FBA_D59
65	BI	FBA_D<60>	V28	FBA_D60
65	BI	FBA_D<61>	V27	FBA_D61
65	BI	FBA_D<62>	V27	FBA_D62
65	BI	FBA_D<63>	V25	FBA_D63

NC	BI CLAMP
GP19	



FBA_CMD0	C27	FBA_CMD0	(U1)	65
FBA_CMD1	C28	FBA_CMD1	(U1)	65
FBA_CMD2	C29	FBA_CMD2	(U1)	65
FBA_CMD3	F20	FBA_CMD3	(U1)	65
FBA_CMD4	U27	FBA_CMD4	(U1)	65
FBA_CMD5	D18	FBA_CMD5	(U1)	65
FBA_CMD6	F20	FBA_CMD6	(U1)	65
FBA_CMD7	F20	FBA_CMD7	(U1)	65
FBA_CMD8	F20	FBA_CMD8	(U1)	65
FBA_CMD9	V25	FBA_CMD9	(U1)	65
FBA_CMD10	U22	FBA_CMD10	(U1)	65
FBA_CMD11	U22	FBA_CMD11	(U1)	65
FBA_CMD12	F27	FBA_CMD12	(U1)	65
FBA_CMD13	U25	FBA_CMD13	(U1)	65
FBA_CMD14	V27	FBA_CMD14	(U1)	65
FBA_CMD15	U26	FBA_CMD15	(U1)	65
FBA_CMD16	N20	FBA_CMD16	(U1)	65
FBA_CMD17	M20	FBA_CMD17	(U1)	65
FBA_CMD18	K24	FBA_CMD18	(U1)	65
FBA_CMD19	N20	FBA_CMD19	(U1)	65
FBA_CMD20	M27	FBA_CMD20	(U1)	65
FBA_CMD21	N20	FBA_CMD21	(U1)	65
FBA_CMD22	M20	FBA_CMD22	(U1)	65
FBA_CMD23	K20	FBA_CMD23	(U1)	65
FBA_CMD24	N20	FBA_CMD24	(U1)	65
FBA_CMD25	J23	FBA_CMD25	(U1)	65
FBA_CMD26	J25	FBA_CMD26	(U1)	65
FBA_CMD27	J25	FBA_CMD27	(U1)	65
FBA_CMD28	K27	FBA_CMD28	(U1)	65
FBA_CMD29	N20	FBA_CMD29	(U1)	65
FBA_CMD30	J27	FBA_CMD30	(U1)	65
FBA_CMD31	J26	FBA_CMD31	(U1)	65

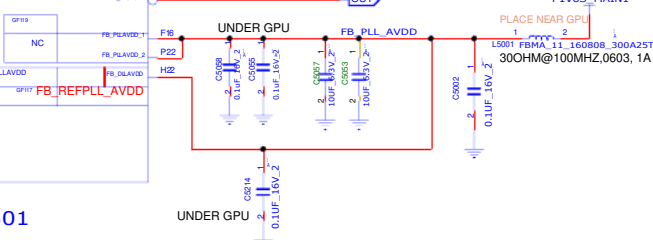
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65	OUT	FBA_DBG1	C17	FBA_DBG1
65	OUT	FBA_DBG2	C17	FBA_DBG2
65	OUT	FBA_DBG3	F24	FBA_DBG3
65	OUT	FBA_DBG4	W20	FBA_DBG4
65	OUT	FBA_DBG5	W20	FBA_DBG5
65	OUT	FBA_DBG6	U25	FBA_DBG6

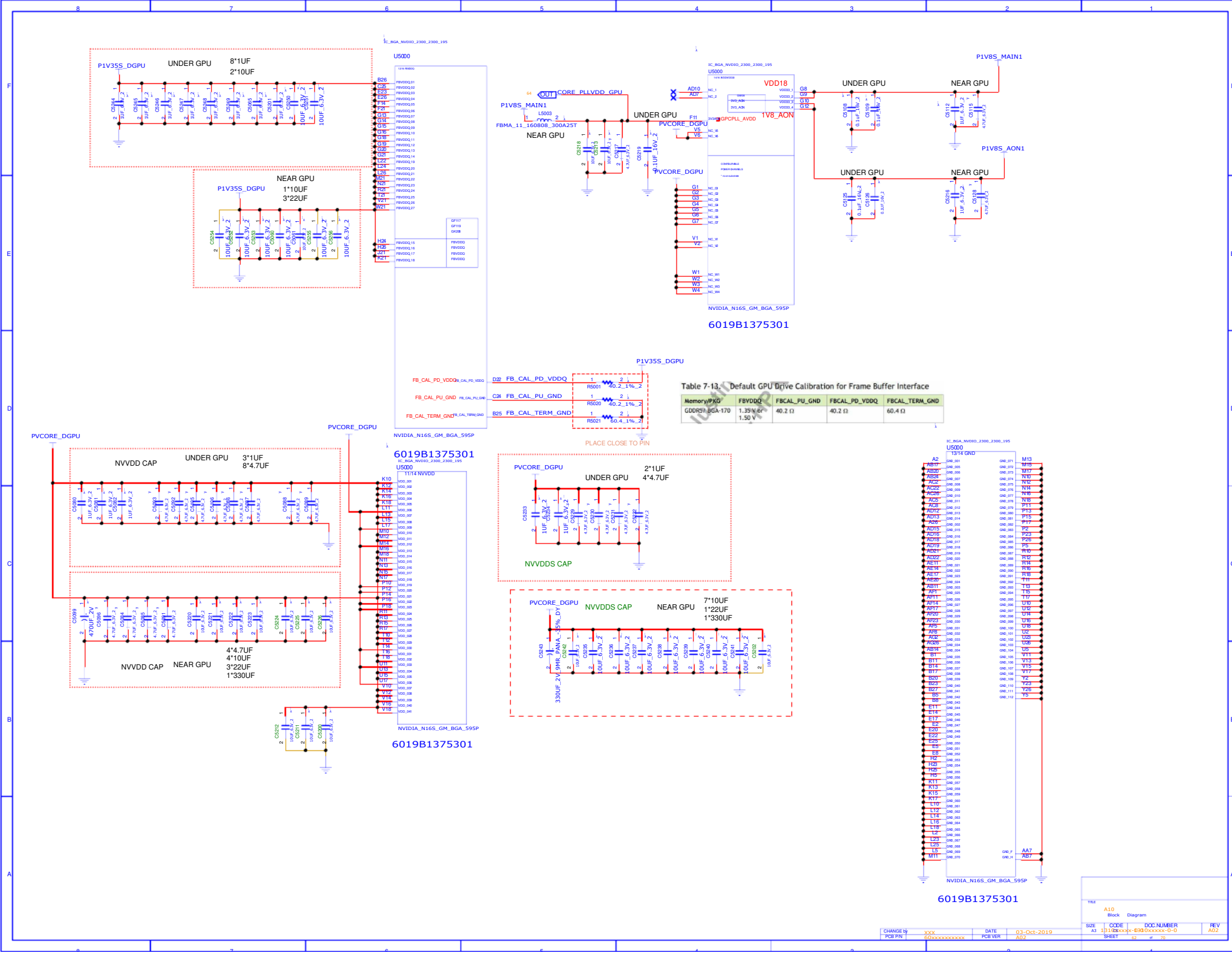
65	OUT	FBA_EDC0	E19	FBA_EDC0
65	OUT	FBA_EDC1	B18	FBA_EDC1
65	OUT	FBA_EDC2	B18	FBA_EDC2
65	OUT	FBA_EDC3	B22	FBA_EDC3
65	OUT	FBA_EDC4	F20	FBA_EDC4
65	OUT	FBA_EDC5	W20	FBA_EDC5
65	OUT	FBA_EDC6	W20	FBA_EDC6
65	OUT	FBA_EDC7	T18	FBA_EDC7

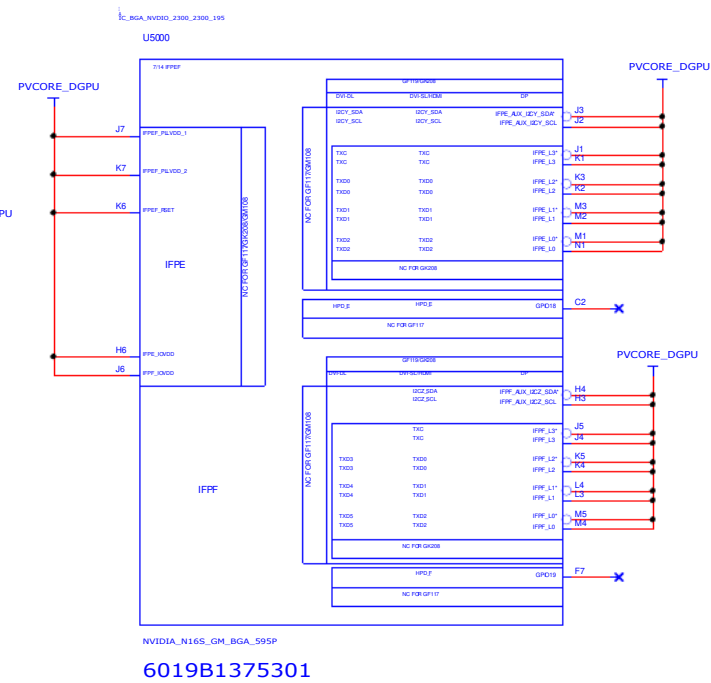
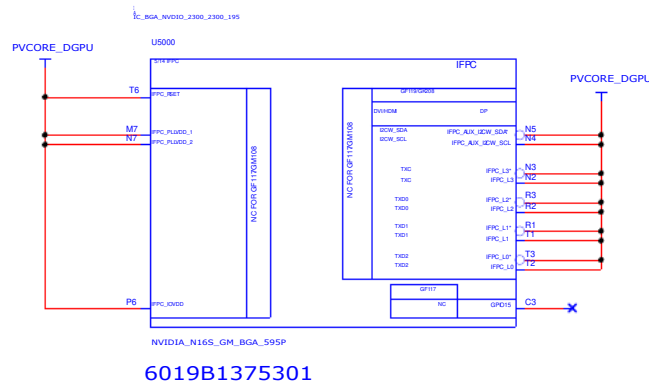
F19	FBA_DBG_R0	
C14	FBA_DBG_R1	
A16	FBA_DBG_R2	
A22	FBA_DBG_R3	
F24	FBA_DBG_R4	
W20	FBA_DBG_R5	
W20	FBA_DBG_R6	
A25	FBA_DBG_R7	
T27	FBA_DBG_R8	

TP24	D20	FBA_DBG_R9
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NVIDIA\_N165\_GM\_BGA\_595P  
6019B1375301







### 5.2.2.3 Assorted Configuration Straps

The following configurable characteristics of the graphics circuit share three physical strap pins:

- SMB\_ALT\_ADDR Enable:** This strap function allows an alternate SMBus address to be configured, so that graphics circuits with multiple GPUs can have separate SMBus connections for each GPU. In dual GPU configurations, use of the alternate address on one GPU (by setting this function to '1') avoids conflicts between the two GPUs on an SMBus port. The "SMB\_ALT\_ADDR Disabled" setting ('0') is correct for single-GPU graphics circuits (see Section 3.3.2.1 for the SMBus address).
- DEVID\_SEL:** NVIDIA defines an original and a re-brand Device ID on a per-GPU basis. This Device ID Select strap function allows selection between the original PCIe Device ID specified for the GPU (via a function setting of '0'), and the alternate "re-brand" Device ID defined for the GPU (via a function setting of '1').
- PCIE\_CFG:** This function sets electrical characteristics of PCIe lanes, in particular signal amplitude (swing). A setting of '0' selects normal (full) signal swing, NVIDIA's graphics circuits should strap for this setting. (A setting of '1' designates reduced signal amplitude, available if special concerns require. Consult NVIDIA for guidance.)
- VGA\_DEVICE:** This strap function is used to report the graphics circuit either as a JD device (class code 302, designated by a setting of '0' for this strap) or as a VGA device (class code 300, designated by a setting of '1') to the host system. The JD Device (class code 302, strap '0') setting is correct for most MS-Hybrid notebook GeForce graphics circuits.

Table 5.6 SMB\_ALT\_ADDR, DEVID\_SEL, PCIE\_CFG, VGA\_DEVICE

Strap Pins		Functions Selected by This Strapping			
STRAP5	STRAP4	STRAP3	SMB_ALT_ADDR	DEVID_SEL	VGA_DEVICE
L	L	L	0	0	0
L	L	H	0	0	1
L	H	L	0	0	1
L	H	H	0	1	1
H	L	L	0	1	0
H	L	H	0	1	0
H	H	L	0	1	0
H	H	H	0	1	1
L	M	L	1	0	0
L	M	H	1	0	1
L	H	M	1	0	1
M	L	L	1	1	0
M	L	H	1	1	0
M	H	L	1	1	0
M	H	H	1	1	1

Table 5.3 RAINCFG

Strap Pins	RAINCFG Setting Number
STRAP2 STRAP1 STRAP0	(see Memory RVL for memory configs corresponding to these numbers)
L L L	0 (0x0000)
L L H	1 (0x0001)
L H L	2 (0x0002)
L H H	3 (0x0003)
H L L	4 (0x0004)
H L H	5 (0x0005)
H H L	6 (0x0006)
H H H	7 (0x0007)
L L M	8 (0x0008)
L H M	9 (0x0009)
L M L	10 (0x000A)
L M H	11 (0x000B)
M L L	12 (0x000C)
M L H	13 (0x000D)

VENDER	DENSITY	VENDER PN	IEC PN	STRAP	STRAP2	STRAP1	STRAP0
SAMSUNG	256MX32	K4G80325FC-HC25(FOR G2)	6019B1912501	0X3	L	H	H
SAMSUNG	256MX32	K4G80325FC-HC25(FOR G5)	6019B1912501	0XB	L	H	M
MICRON	256MX32	MT51J256M32HF-80-B	6019B1912401	0X9	L	M	L
HYNIX	256MX32	H5GC8H24AJR-R2C	6019B1878601	0XA	L	M	H

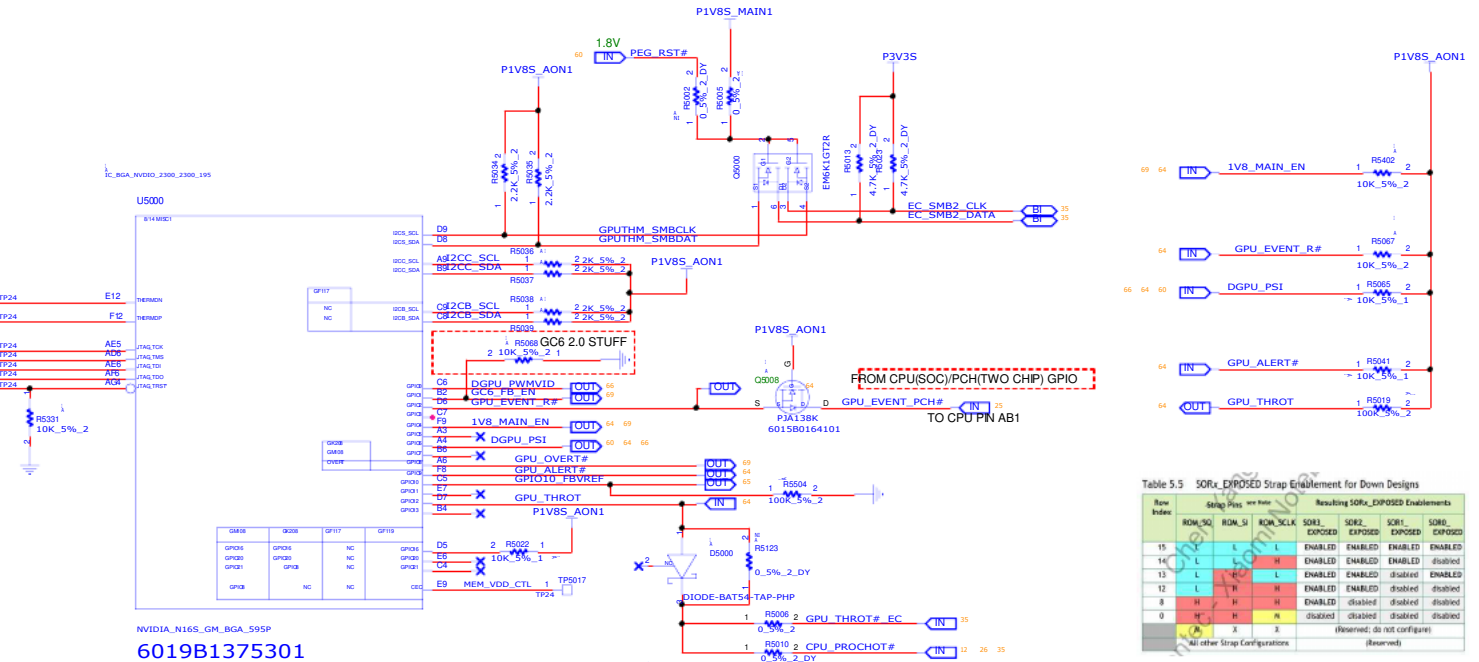
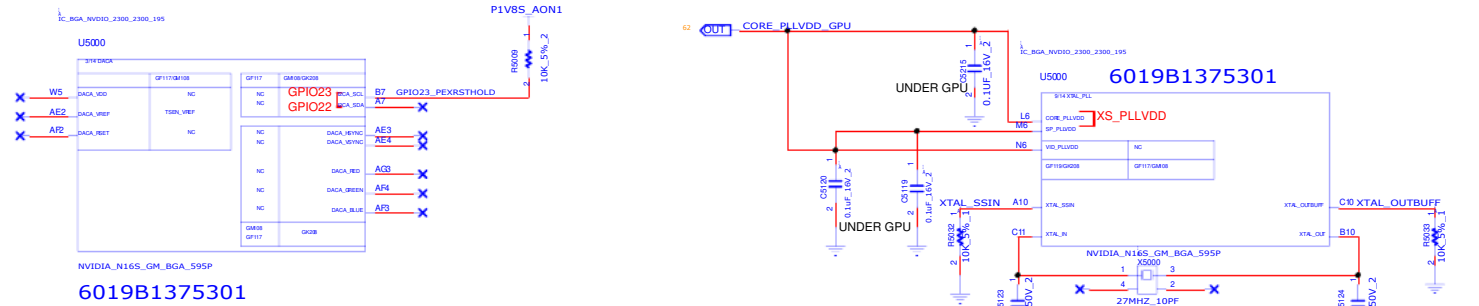
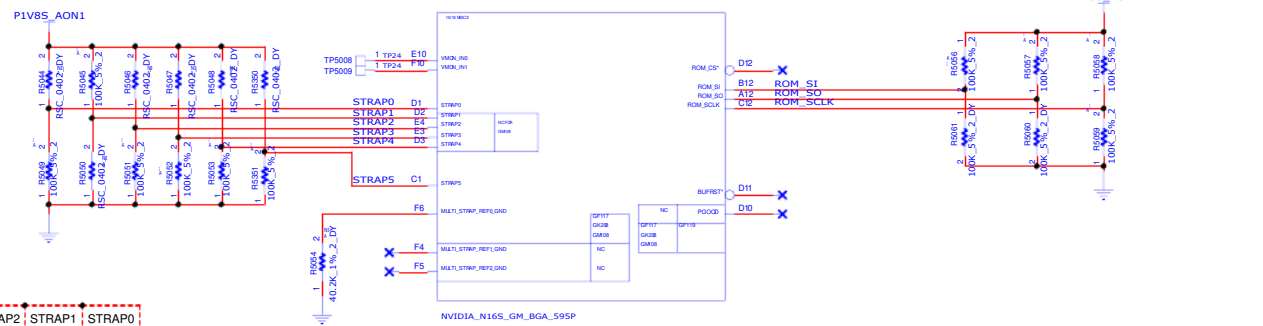
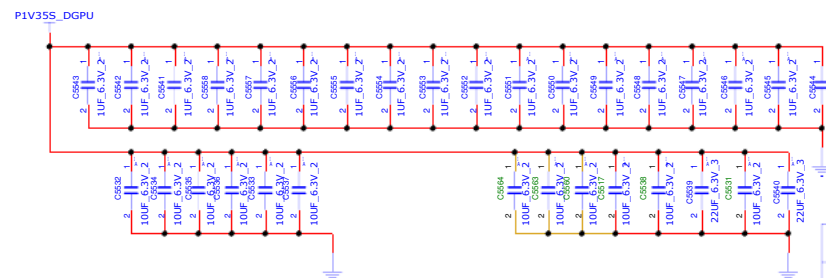
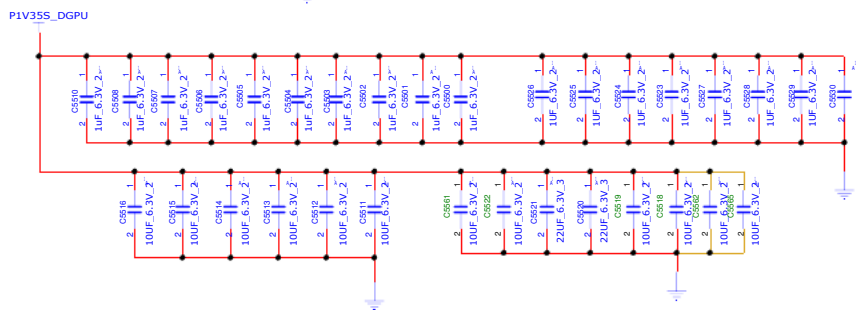
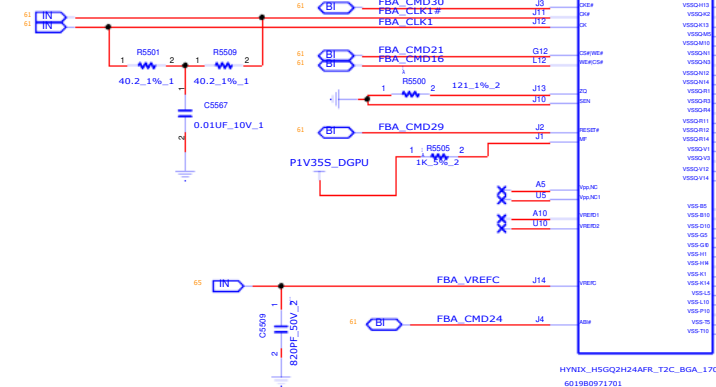
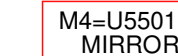


Table 5.5 SORA-EXPOSED Strap Enablement for Down Designs										
Row Index	Strap Pins we have				Resulting SORA-EXPOSED Enablements					
	ROM_S0	ROM_S1	ROM_S2	ROM_S3	SORA1 EXPOSED	SORA2 EXPOSED	SORA3 EXPOSED	SORA4 EXPOSED	SORA5 EXPOSED	
15	L	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED	ENABLED	
14	L	L	L	L	ENABLED	ENABLED	ENABLED	ENABLED	disabled	
13	L	L	L	L	ENABLED	ENABLED	disabled	disabled	ENABLED	
12	L	L	L	L	ENABLED	ENABLED	disabled	disabled	disabled	
8	H	H	H	H	ENABLED	disabled	disabled	disabled	disabled	
0	H	H	H	H	disabled	disabled	disabled	disabled	disabled	
	L	X	X	X	(disabled; do not configure)					
	All other Strap Configurations				(Reserved)					





M3=U5500  
NON MIRROR

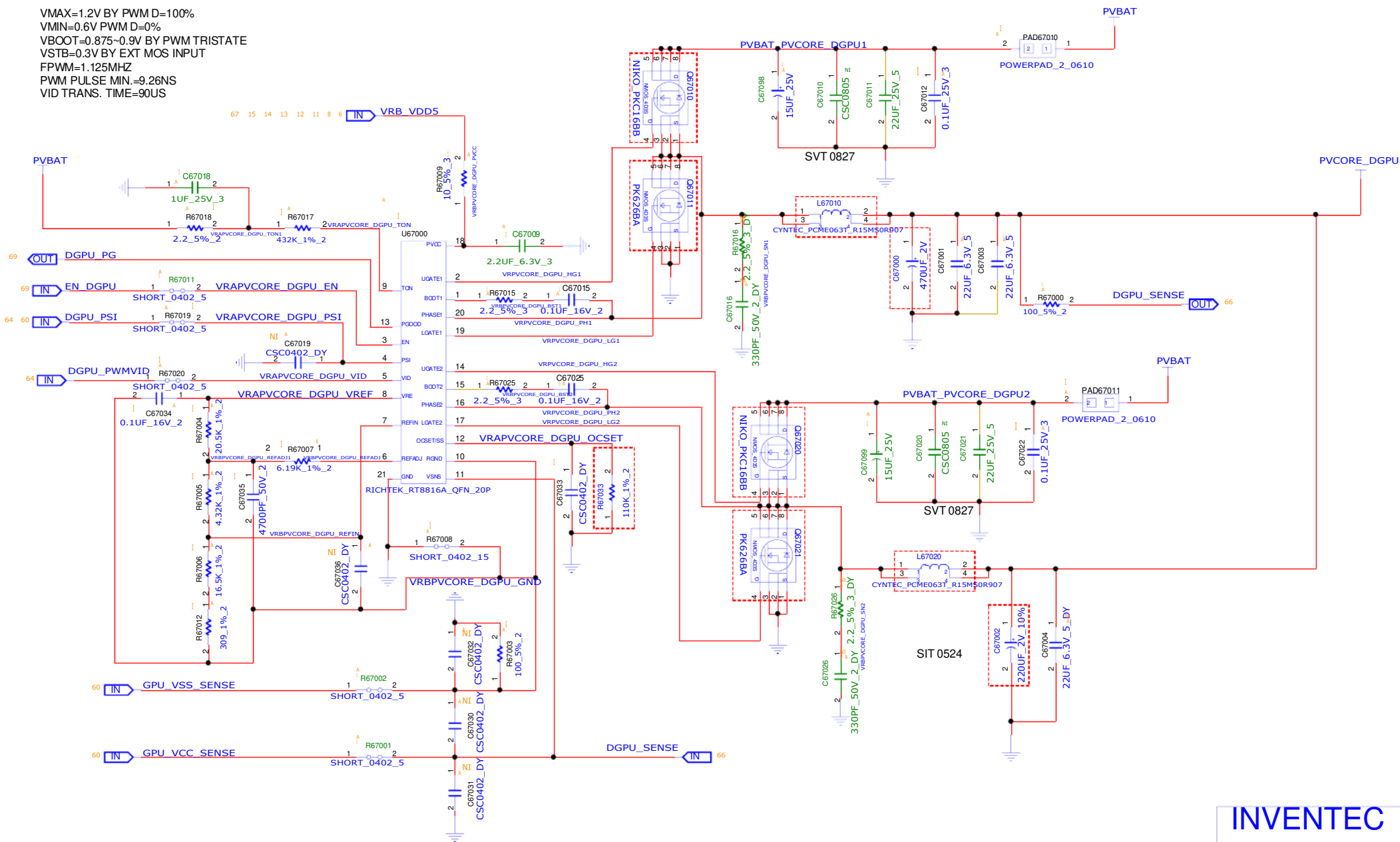


INVENTEC

TITLE		
A10 Block Diagram		
SIZE C	CODE CS	DOC NUMBER 1310xxxxxx-0-0
SHEET of 65 70		

CHANGE BY	XXX	DATE	SIZE	CODE	DOC NUMBER
PCB P/N	60-8153-0000	PCB VER	C	CS	1310xxxxxx-0-0
03-Oct-2019			SHEET		
			of 65 70		

VMAX=1.2V BY PWM D=100%  
 VMIN=0.6V PWM D=0%  
 VBOOT=0.875~0.9V BY PWM TRISTATE  
 VSTB=0.3V BY EXT MOS INPUT  
 FPWM=1.125MHZ  
 PWM PULSE MIN.=9.26NS  
 VID TRANS. TIME=90US



INVENTEC

TITLE				
A10 Block Diagram				
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SHEET	66	of 70		

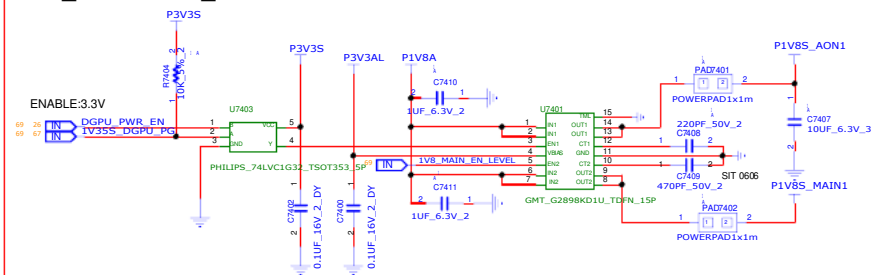
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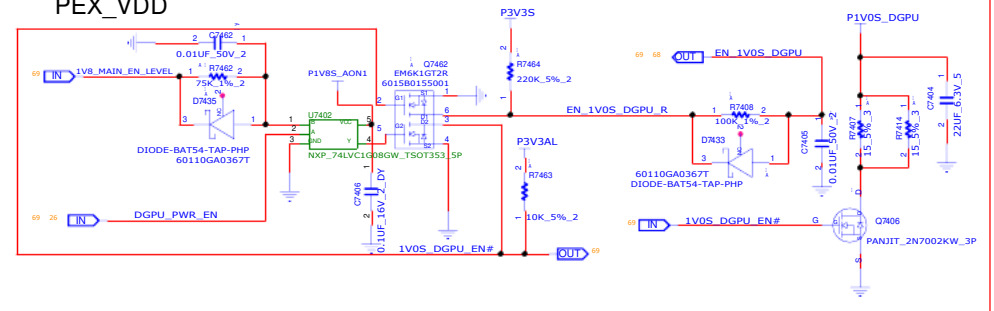


POWER\_ON: P1V8S\_AON1-->P1V8S\_MAIN1-->NVVDD-->PEX\_VDD-->FBVDD  
POWER\_OFF:FBVDD-->PEX\_VDD-->NVVDD-->P1V8S\_MAIN1-->P1V8S\_AON1

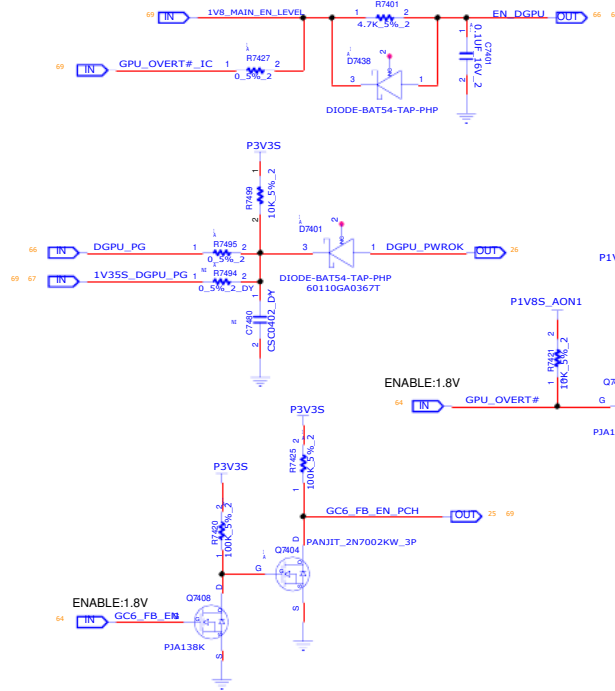
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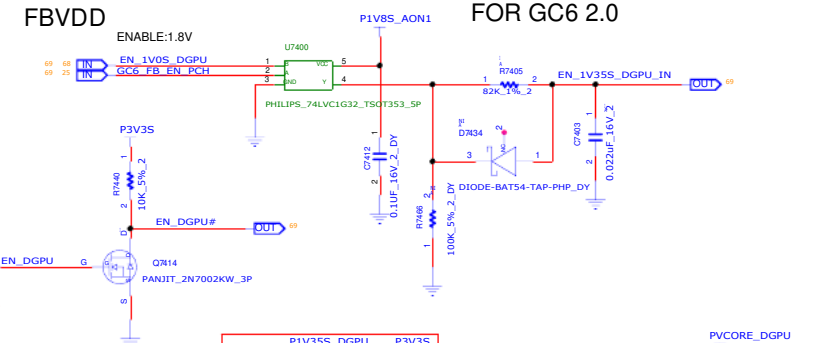
## PEX\_VDD



## NVVDD

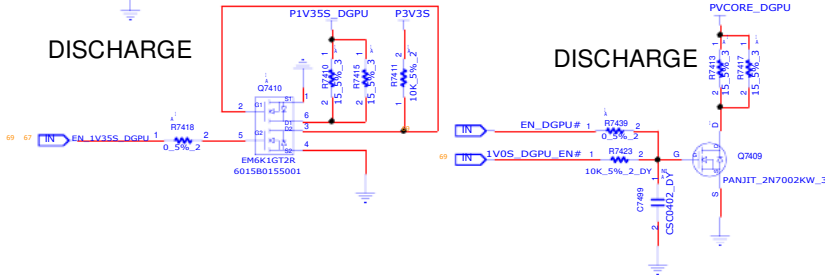


## FBVDD



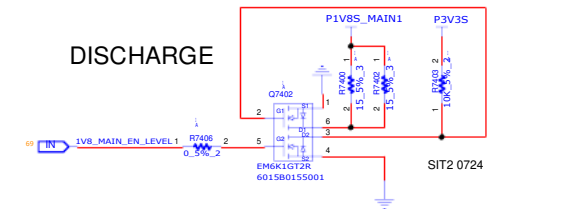
FOR GC6 2.0

## DISCHARGE

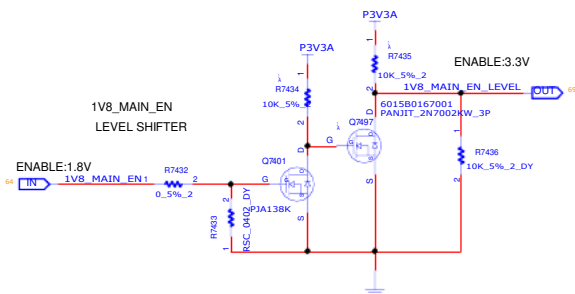
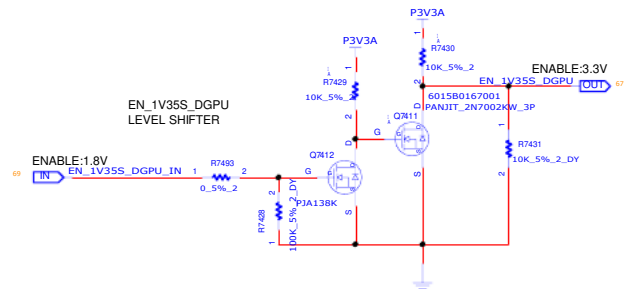


## DISCHARGE

## DISCHARGE



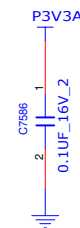
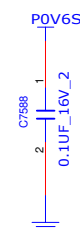
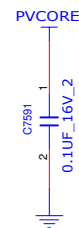
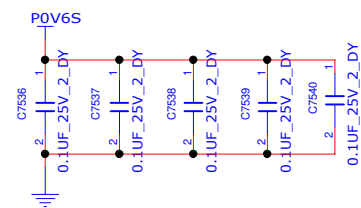
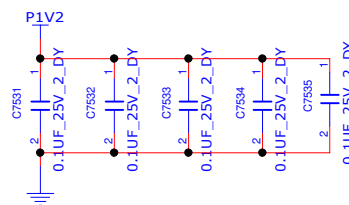
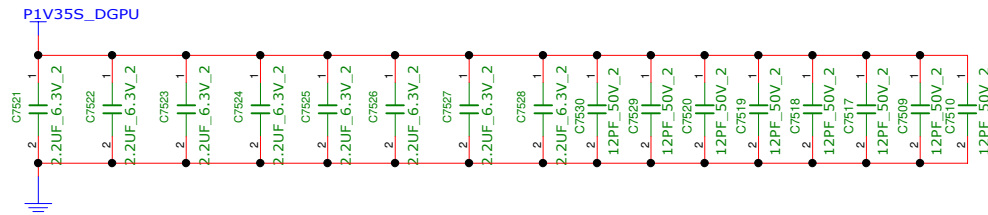
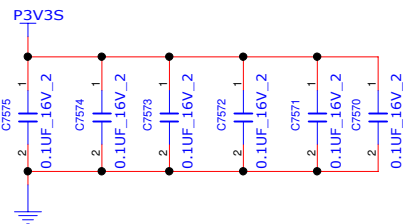
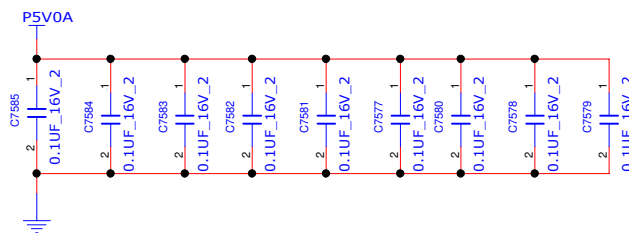
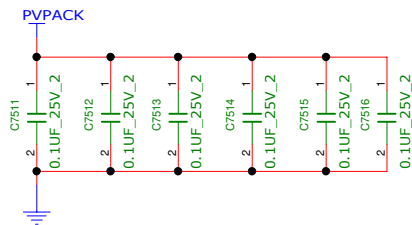
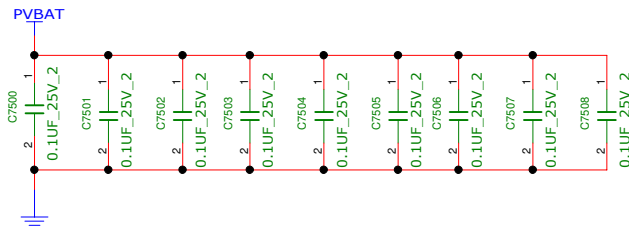
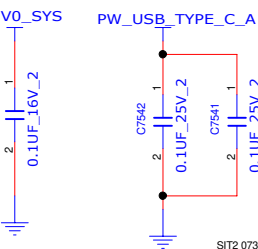
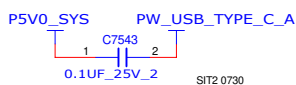
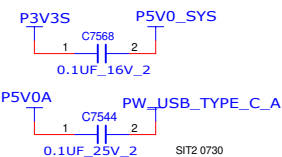
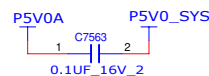
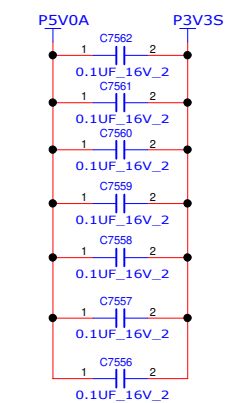
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LEVEL SHIFTER

EN\_1V35S\_DGPU  
LEVEL SHIFTER

INVENTEC

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# RF&EMI



INVENTEC			
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SHEET		70 of 70	

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